

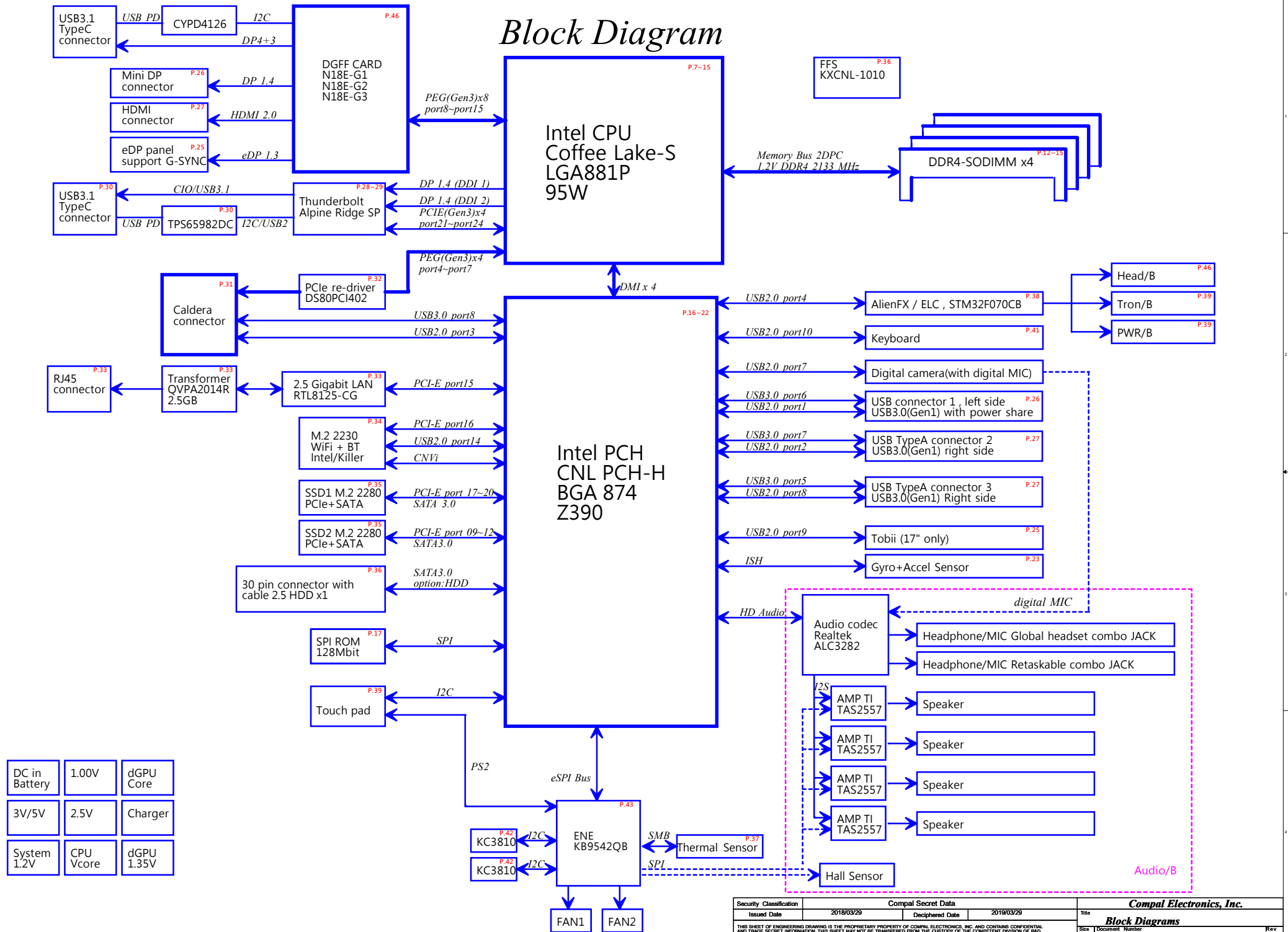
LA-G881P Coffee Lake-S 95W CNL PCH-H with nVIDIA N18E

REV : 1.0
2018.12.14

@ : Nopop Component
EMI@,ESD@,RF@ : EMI/ESD/RF part
CONN@ : Connector Component
@EMI@,@ESD@,@RF@ : Total debug Component
CNVI@:For WLAN
NOCP@/OCP@:For Hinge up OCP

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2018/03/29	Deciphered Date	2019/03/29	Title		
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Block Diagram



Voc	0.50 +/- 1%				
Ra	250K +/- 1%				
Lead In	Rb	Vas size	Vas size	Vas size	Vas size
		Min	Max	typ	Min
0	0	0.000V	0.000V	0.000V	0.000V
1	22K +/- 1%	0.347V	0.354V	0.060V	0.013
2	33K +/- 1%	0.423V	0.430V	0.065V	0.018
3	50K +/- 1%	0.541V	0.550V	0.065V	0.025
4	67K +/- 1%	0.691V	0.702V	0.065V	0.030
5	82K +/- 1%	0.807V	0.819V	0.063V	0.03A
6	100K +/- 1%	0.978V	0.992V	0.064V	0.045
7	150K +/- 1%	1.265V	1.281V	0.064V	0.064
8	220K +/- 1%	1.398V	1.414V	0.065V	0.075
9	300K +/- 1%	1.534V	1.650V	0.067V	0.087

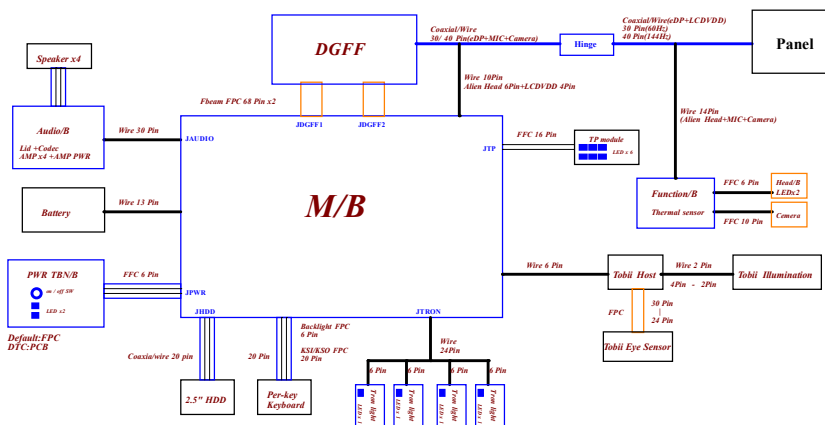
NV	PCB Revision
0	EVT
1	DVT-1
2	DVT-2
3	Pilot

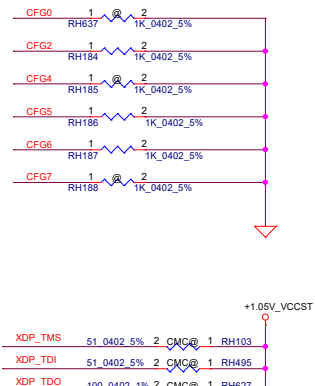
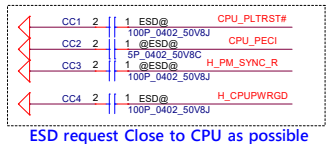
[illegible]

HSIO	USB3.1	PCIe	SATA3	Function
0	1			
1	2			
2	3			
3	4			
4	5			USB3
5	6			USB1(Powershare)
6	7	1		USB2
7	8	2		Catdera
8	9	3		
9	10	4		
10	5			
11	6			
12	7			
13	8			
14	9			
15	10			
16	11	0a		JSSD2 , 2280 SATA/PCIe x4
17	12	1a		
18	13	0b		JHDD
19	14	1b		
20	15	2		LAN
21	16	3		WLAN
22	17	4		
23	18	5		
24	19			JSSD1 , 2280 SATA/PCIe x4
25	20			
26	21			
27	22			
28	23			Thunderbolt
29	24			

USB2	Function
1	JUSB1 (Powershare)
2	JUSB2
3	Caldera
4	ELC
5	
6	
7	Camera
8	JUSB3
9	Tobii
10	Per-key
11	Thunderbolt PD
12	
13	
14	Bluetooth

 *Digital Ground*
 *Analog Ground*



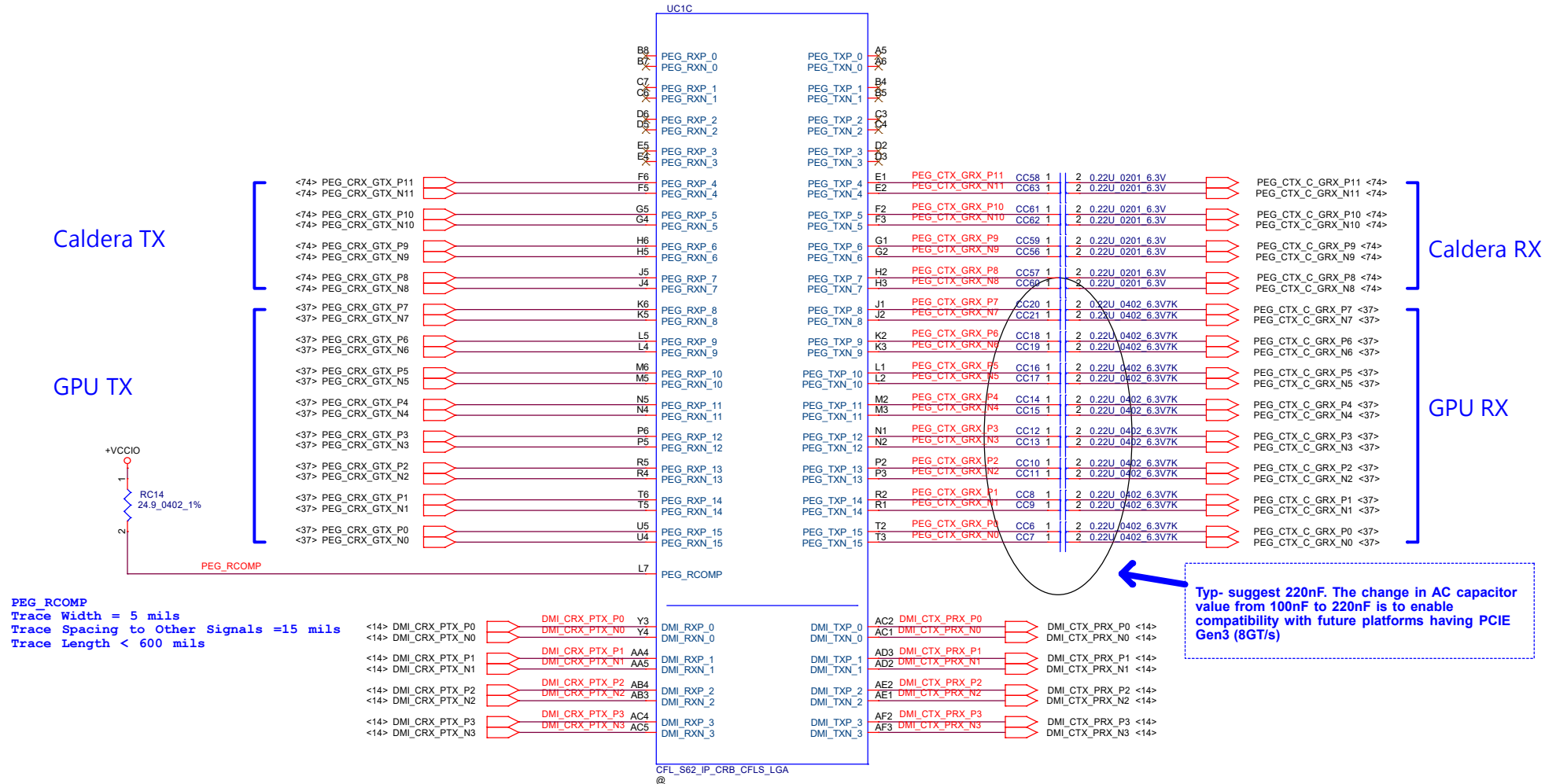


PEG DEFER TRAINING	
CFG7	<p>★ 1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

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				CFL-S JTAG/XDP/DDI	
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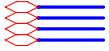
Table 2-13. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes															
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 Reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 Reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0



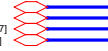
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<23.25> DDR_A_DQ[0..63]
<23.25> DDR_A_MA[0..15]
<23.25> DDR_A_DQS#[0..7]
<23.25> DDR_A_DQS0[0..7]



Channel A

<24.25> DDR_B_DQ[0..63]
<24.25> DDR_B_MA[0..15]
<24.25> DDR_B_DQS#[0..7]
<24.25> DDR_B_DQS0[0..7]



Channel B

UC1A

DDR_A_D0	AE38	DDR0_DQ_0/DDR0_DQ_0	DDR0_CKP_0	AW18	DDR_A_CLK0 <25>	
DDR_A_D1	AE37	DDR0_DQ_1/DDR0_DQ_1	DDR0_CKN_0	AW18	DDR_A_CLK#0 <25>	
DDR_A_D2	AG38	DDR0_DQ_2/DDR0_DQ_2	DDR0_CKP_1	AW17	DDR_A_CLK1 <25>	
DDR_A_D3	AG37	DDR0_DQ_3/DDR0_DQ_3	DDR0_CKN_1	AW17	DDR_A_CLK#1 <25>	
DDR_A_D4	AE39	DDR0_DQ_4/DDR0_DQ_4	DDR0_CKP_2	AW16	DDR_A_CLK2 <25>	
DDR_A_D5	AE40	DDR0_DQ_5/DDR0_DQ_5	DDR0_CKN_2	AW16	DDR_A_CLK#2 <25>	
DDR_A_D6	AG39	DDR0_DQ_6/DDR0_DQ_6	DDR0_CKP_3	AW16	DDR_A_CLK3 <25>	
DDR_A_D7	AG40	DDR0_DQ_7/DDR0_DQ_7	DDR0_CKN_3	AW16	DDR_A_CLK#3 <25>	
DDR_A_D8	AJ38	DDR0_DQ_8/DDR0_DQ_8				
DDR_A_D9	AJ37	DDR0_DQ_9/DDR0_DQ_9				
DDR_A_D10	AL38	DDR0_DQ_10/DDR0_DQ_10	DDR0_CKE_0	AW24	DDR_A_CKE0 <25>	
DDR_A_D11	AL37	DDR0_DQ_11/DDR0_DQ_11	DDR0_CKE_1	AW24	DDR_A_CKE1 <25>	
DDR_A_D12	AJ40	DDR0_DQ_12/DDR0_DQ_12	DDR0_CKE_2	AW25	DDR_A_CKE2 <25>	
DDR_A_D13	AJ39	DDR0_DQ_13/DDR0_DQ_13	DDR0_CKE_3	AW25	DDR_A_CKE3 <25>	
DDR_A_D14	AL39	DDR0_DQ_14/DDR0_DQ_14				
DDR_A_D15	AL40	DDR0_DQ_15/DDR0_DQ_15	DDR0_CSW_0	AW12	DDR_A_CSW0 <25>	
DDR_A_D16	AK38	DDR0_DQ_16/DDR0_DQ_16	DDR0_CSW_1	AU11	DDR_A_CSW1 <25>	
DDR_A_D17	AK39	DDR0_DQ_17/DDR0_DQ_17	DDR0_CSW_2	AU13	DDR_A_CSW2 <25>	
DDR_A_D18	AR38	DDR0_DQ_18/DDR0_DQ_18	DDR0_CSW_3	AV10	DDR_A_CSW3 <25>	
DDR_A_D19	AR37	DDR0_DQ_19/DDR0_DQ_19				
DDR_A_D20	AN39	DDR0_DQ_20/DDR0_DQ_20	DDR0_ODT_0	AW11	DDR_A_ODT0 <25>	
DDR_A_D21	AN37	DDR0_DQ_21/DDR0_DQ_21	DDR0_ODT_1	AU14	DDR_A_ODT1 <25>	
DDR_A_D22	AR39	DDR0_DQ_22/DDR0_DQ_22	DDR0_ODT_2	AU12	DDR_A_ODT2 <25>	
DDR_A_D23	AR40	DDR0_DQ_23/DDR0_DQ_23	DDR0_ODT_3	AY10	DDR_A_ODT3 <25>	
DDR_A_D24	AW37	DDR0_DQ_24/DDR0_DQ_24				
DDR_A_D25	AU38	DDR0_DQ_25/DDR0_DQ_25	DDR0_BA_0	AY13	DDR_A_BA0 <23.25>	
DDR_A_D26	AW36	DDR0_DQ_26/DDR0_DQ_26	DDR0_BA_1	AY15	DDR_A_BA1 <23.25>	
DDR_A_D27	AW35	DDR0_DQ_27/DDR0_DQ_27	DDR0_BG_0	AW23	DDR_A_BG0 <23.25>	
DDR_A_D28	AU37	DDR0_DQ_28/DDR0_DQ_28				
DDR_A_D29	AY37	DDR0_DQ_29/DDR0_DQ_29	DDR0_MA_16	AW13	DDR_A_RAS# <23.25>	
DDR_A_D30	AY35	DDR0_DQ_30/DDR0_DQ_30	DDR0_MA_14	AY14	DDR_A_WE# <23.25>	
DDR_A_D31	AU35	DDR0_DQ_31/DDR0_DQ_31	DDR0_MA_15	AY11	DDR_A_CAS# <23.25>	
DDR_A_D32	AY36	DDR0_DQ_32/DDR0_DQ_32				
DDR_A_D33	AW38	DDR0_DQ_33/DDR0_DQ_33	DDR0_MA_0	AW15	DDR_A_MA0 <23.25>	
DDR_A_D34	AW36	DDR0_DQ_34/DDR0_DQ_34	DDR0_MA_1	AU18	DDR_A_MAT0 <23.25>	
DDR_A_D35	AU36	DDR0_DQ_35/DDR0_DQ_35	DDR0_MA_2	AU17	DDR_A_MAT1 <23.25>	
DDR_A_D36	AU35	DDR0_DQ_36/DDR0_DQ_36	DDR0_MA_3	AU19	DDR_A_MAT2 <23.25>	
DDR_A_D37	AW38	DDR0_DQ_37/DDR0_DQ_37	DDR0_MA_4	AT19	DDR_A_MAT3 <23.25>	
DDR_A_D38	AW36	DDR0_DQ_38/DDR0_DQ_38	DDR0_MA_5	AU20	DDR_A_MAT4 <23.25>	
DDR_A_D39	AW35	DDR0_DQ_39/DDR0_DQ_39	DDR0_MA_6	AU20	DDR_A_MAT5 <23.25>	
DDR_A_D40	AY34	DDR0_DQ_40/DDR0_DQ_40	DDR0_MA_7	AU21	DDR_A_MAT6 <23.25>	
DDR_A_D41	AY34	DDR0_DQ_41/DDR0_DQ_41	DDR0_MA_8	AT20	DDR_A_MAT7 <23.25>	
DDR_A_D42	AT11	DDR0_DQ_42/DDR0_DQ_42	DDR0_MA_9	AT22	DDR_A_MAT8 <23.25>	
DDR_A_D43	AT12	DDR0_DQ_43/DDR0_DQ_43	DDR0_MA_10	AT22	DDR_A_MAT9 <23.25>	
DDR_A_D44	AV3	DDR0_DQ_44/DDR0_DQ_44	DDR0_MA_11	AY14	DDR_A_MAT10 <23.25>	
DDR_A_D45	AW4	DDR0_DQ_45/DDR0_DQ_45	DDR0_MA_12	AU22	DDR_A_MAT11 <23.25>	
DDR_A_D46	AT14	DDR0_DQ_46/DDR0_DQ_46	DDR0_MA_13	AT22	DDR_A_MAT12 <23.25>	
DDR_A_D47	AT13	DDR0_DQ_47/DDR0_DQ_47	DDR0_BG_1	AV23	DDR_A_BG1 <23.25>	
DDR_A_D48	AP2	DDR0_DQ_48/DDR0_DQ_48	DDR0_ACT#	AU24	DDR_A_ACT# <23.25>	
DDR_A_D49	AM	DDR0_DQ_49/DDR0_DQ_49				
DDR_A_D50	AP3	DDR0_DQ_50/DDR0_DQ_50	DDR0_PAR	AY15	DDR_A_PAR <23.25>	
DDR_A_D51	AM3	DDR0_DQ_51/DDR0_DQ_51	DDR0_ALERT#	AT23	DDR_A_ALERT# <23.25>	
DDR_A_D52	AF4	DDR0_DQ_52/DDR0_DQ_52				
DDR_A_D53	AM2	DDR0_DQ_53/DDR0_DQ_53				
DDR_A_D54	AM1	DDR0_DQ_54/DDR0_DQ_54				
DDR_A_D55	AK3	DDR0_DQ_55/DDR0_DQ_55				
DDR_A_D56	AK4	DDR0_DQ_56/DDR0_DQ_56				
DDR_A_D57	AK5	DDR0_DQ_57/DDR0_DQ_57				
DDR_A_D58	AK6	DDR0_DQ_58/DDR0_DQ_58				
DDR_A_D59	AK7	DDR0_DQ_59/DDR0_DQ_59				
DDR_A_D60	AK8	DDR0_DQ_60/DDR0_DQ_60				
DDR_A_D61	AK9	DDR0_DQ_61/DDR0_DQ_61				
DDR_A_D62	AK10	DDR0_DQ_62/DDR0_DQ_62				
DDR_A_D63	AK11	DDR0_DQ_63/DDR0_DQ_63				

DDR CHANNEL A

CFL_S62_IP_CRB_CFLS_LGA

UC1B

DDR_B_D0	AD34	DDR1_DQ_0/DDR0_DQ_16	DDR1_CKP_0	AM20	DDR_B_CLK0 <26>	
DDR_B_D1	AD35	DDR1_DQ_1/DDR0_DQ_17	DDR1_CKN_0	AM21	DDR_B_CLK#0 <26>	
DDR_B_D2	AG35	DDR1_DQ_2/DDR0_DQ_18	DDR1_CKP_1	AP22	DDR_B_CLK#1 <26>	
DDR_B_D3	AG36	DDR1_DQ_3/DDR0_DQ_19	DDR1_CKN_1	AN20	DDR_B_CLK#2 <26>	
DDR_B_D4	AE35	DDR1_DQ_4/DDR0_DQ_20	DDR1_CKP_2	AN21	DDR_B_CLK#3 <26>	
DDR_B_D5	AE34	DDR1_DQ_5/DDR0_DQ_21	DDR1_CKN_2	AP19	DDR_B_CLK#4 <26>	
DDR_B_D6	AG34	DDR1_DQ_6/DDR0_DQ_22	DDR1_CKP_3	AP20	DDR_B_CLK#5 <26>	
DDR_B_D7	AH34	DDR1_DQ_7/DDR0_DQ_23	DDR1_CKN_3	AY29	DDR_B_CKE0 <26>	
DDR_B_D8	AK35	DDR1_DQ_8/DDR0_DQ_24				
DDR_B_D9	AL35	DDR1_DQ_9/DDR0_DQ_25	DDR1_CKE_0	AW29	DDR_B_CKE1 <26>	
DDR_B_D10	AK32	DDR1_DQ_10/DDR0_DQ_26	DDR1_CKE_1	AU29	DDR_B_CKE2 <26>	
DDR_B_D11	AL32	DDR1_DQ_11/DDR0_DQ_27	DDR1_CKE_2			
DDR_B_D12	AK34	DDR1_DQ_12/DDR0_DQ_28	DDR1_CKE_3			
DDR_B_D13	AL34	DDR1_DQ_13/DDR0_DQ_29				
DDR_B_D14	AK31	DDR1_DQ_14/DDR0_DQ_30	DDR1_CSW_0	AP17	DDR_B_CSW0 <26>	
DDR_B_D15	AL31	DDR1_DQ_15/DDR0_DQ_31	DDR1_CSW_1	AN15	DDR_B_CSW1 <26>	
DDR_B_D16	AP35	DDR1_DQ_16/DDR0_DQ_32	DDR1_CSW_2	AM15	DDR_B_CSW2 <26>	
DDR_B_D17	AN35	DDR1_DQ_17/DDR0_DQ_33	DDR1_CSW_3	AM16	DDR_B_CSW3 <26>	
DDR_B_D18	AN32	DDR1_DQ_18/DDR0_DQ_34	DDR1_ODT_0	AL16	DDR_B_ODT0 <26>	
DDR_B_D19	AP32	DDR1_DQ_19/DDR0_DQ_35	DDR1_ODT_1	AP15	DDR_B_ODT1 <26>	
DDR_B_D20	AK34	DDR1_DQ_20/DDR0_DQ_36	DDR1_ODT_2	AL15	DDR_B_ODT2 <26>	
DDR_B_D21	AP34	DDR1_DQ_21/DDR0_DQ_37	DDR1_ODT_3			
DDR_B_D22	AK31	DDR1_DQ_22/DDR0_DQ_38				
DDR_B_D23	AP31	DDR1_DQ_23/DDR0_DQ_39				
DDR_B_D24	AL29	DDR1_DQ_24/DDR0_DQ_40	DDR1_MA_16	AN18	DDR_B_RAS# <24.26>	
DDR_B_D25	AM29	DDR1_DQ_25/DDR0_DQ_41	DDR1_MA_15	AL17	DDR_B_WE# <24.26>	
DDR_B_D26	AP29	DDR1_DQ_26/DDR0_DQ_42		AP16	DDR_B_CAS# <24.26>	
DDR_B_D27	AR29	DDR1_DQ_27/DDR0_DQ_43				
DDR_B_D28	AM28	DDR1_DQ_28/DDR0_DQ_44	DDR1_BA_0	AL18	DDR_B_BA0 <24.26>	
DDR_B_D29	AL28	DDR1_DQ_29/DDR0_DQ_45	DDR1_BA_1	AW28	DDR_B_BA1 <24.26>	
DDR_B_D30	AR28	DDR1_DQ_30/DDR0_DQ_46	DDR1_BG_0		DDR_B_BG0 <24.26>	
DDR_B_D31	AP28	DDR1_DQ_31/DDR0_DQ_47				
DDR_B_D32	AK22	DDR1_DQ_32/DDR0_DQ_48	DDR1_MA_0	AL19	DDR_B_MA0 <24.26>	
DDR_B_D33	AP12	DDR1_DQ_33/DDR0_DQ_49	DDR1_MA_1	AL22	DDR_B_MAT0 <24.26>	
DDR_B_D34	AM13	DDR1_DQ_34/DDR0_DQ_50	DDR1_MA_2	AM22	DDR_B_MAT1 <24.26>	
DDR_B_D35	AL13	DDR1_DQ_35/DDR0_DQ_51	DDR1_MA_3	AM23	DDR_B_MAT2 <24.26>	
DDR_B_D36	AR13	DDR1_DQ_36/DDR0_DQ_52	DDR1_MA_4	AP23	DDR_B_MAT3 <24.26>	
DDR_B_D37	AP13	DDR1_DQ_37/DDR0_DQ_53	DDR1_MA_5	AL23	DDR_B_MAT4 <24.26>	
DDR_B_D38	AL12	DDR1_DQ_38/DDR0_DQ_54	DDR1_MA_6	AW26	DDR_B_MAT5 <24.26>	
DDR_B_D39	AP10	DDR1_DQ_39/DDR0_DQ_55	DDR1_MA_7	AY26	DDR_B_MAT6 <24.26>	
DDR_B_D40	AR10	DDR1_DQ_40/DDR0_DQ_56	DDR1_MA_8	AW27	DDR_B_MAT7 <24.26>	
DDR_B_D41	AP10	DDR1_DQ_41/DDR0_DQ_57	DDR1_MA_9	AP18	DDR_B_MAT8 <24.26>	
DDR_B_D42	AR1	DDR1_DQ_42/DDR0_DQ_58	DDR1_MA_10	AU27	DDR_B_MAT9 <24.26>	
DDR_B_D43	AP7	DDR1_DQ_43/DDR0_DQ_59	DDR1_MA_11	AV27	DDR_B_MAT10 <24.26>	
DDR_B_D44	AR9	DDR1_DQ_44/DDR0_DQ_60	DDR1_MA_12	AR15	DDR_B_MAT11 <24.26>	
DDR_B_D45	AP9	DDR1_DQ_45/DDR0_DQ_61	DDR1_MA_13	AY28	DDR_B_BG1 <24.26>	
DDR_B_D46	AR8	DDR1_DQ_46/DDR0_DQ_62	DDR1_BG_1	AU28	DDR_B_ACT# <24.26>	
DDR_B_D47	AP8	DDR1_DQ_47/DDR0_DQ_63				
DDR_B_D48	AL10	DDR1_DQ_48/DDR0_DQ_64	DDR1_PAR	AL20	DDR_B_PAR <24.26>	
DDR_B_D49	AM7	DDR1_DQ_49/DDR0_DQ_65	DDR1_ALERT#	AY25	DDR_B_ALERT# <24.26>	
DDR_B_D50	AL7	DDR1_DQ_50/DDR0_DQ_66				
DDR_B_D51	AM6	DDR1_DQ_51/DDR0_DQ_67				
DDR_B_D52	AL9	DDR1_DQ_52/DDR0_DQ_68				
DDR_B_D53	AM5	DDR1_DQ_53/DDR0_DQ_69				
DDR_B_D54	AL6	DDR1_DQ_54/DDR0_DQ_70				
DDR_B_D55	AJ6	DDR1_DQ_55/DDR0_DQ_71				
DDR_B_D56	AJ7	DDR1_DQ_56/DDR0_DQ_72				
DDR_B_D57	AE8	DDR1_DQ_57/DDR0_DQ_73				
DDR_B_D58	AE7	DDR1_DQ_58/DDR0_DQ_74				
DDR_B_D59	AH7	DDR1_DQ_59/DDR0_DQ_75				
DDR_B_D60	AE7	DDR1_DQ_60/DDR0_DQ_76				
DDR_B_D61	AE7	DDR1_DQ_61/DDR0_DQ_77				
DDR_B_D62	AE7	DDR1_DQ_62/DDR0_DQ_78				
DDR_B_D63	AE7	DDR1_DQ_63/DDR0_DQ_79				

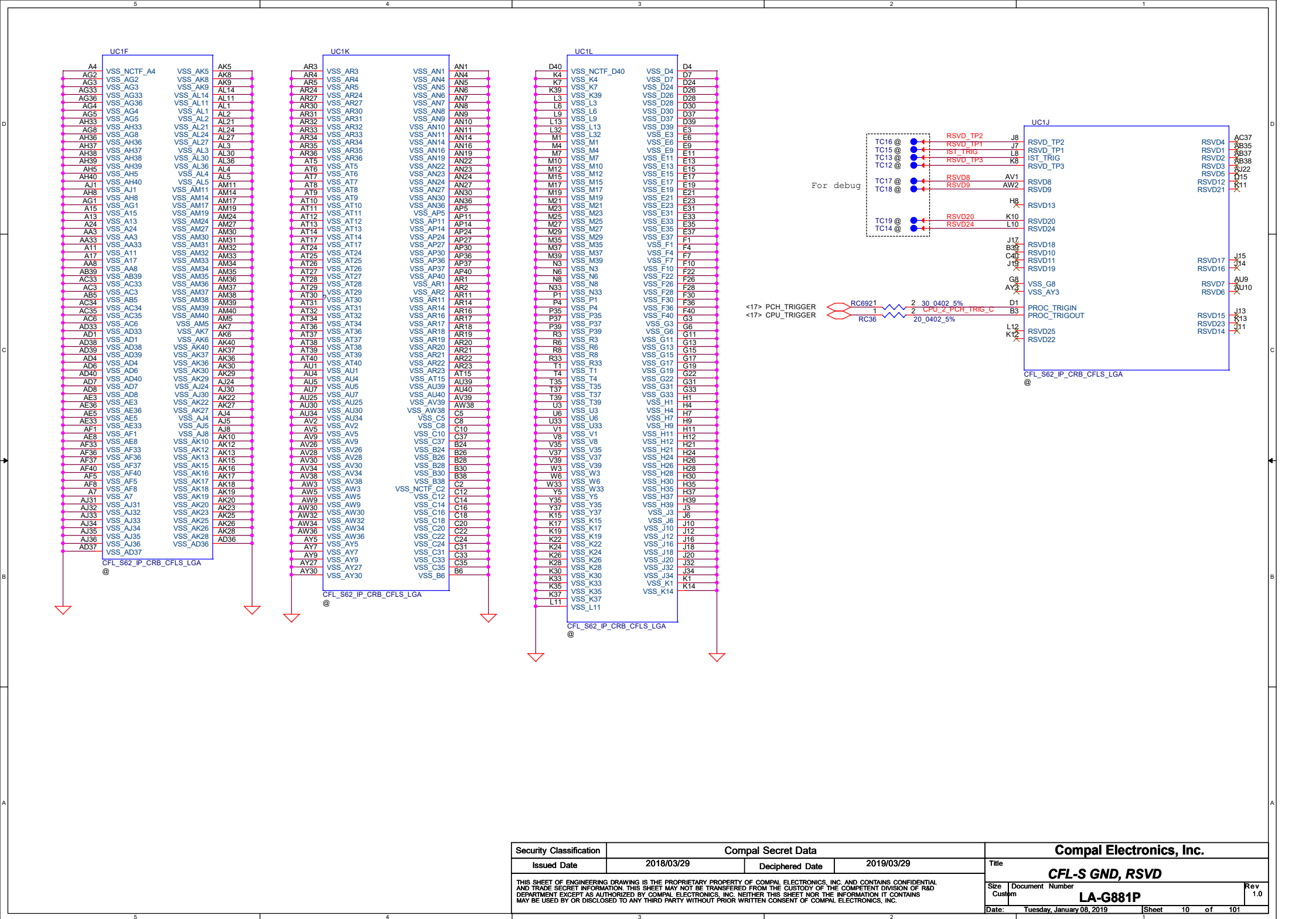
DDR CHANNEL B

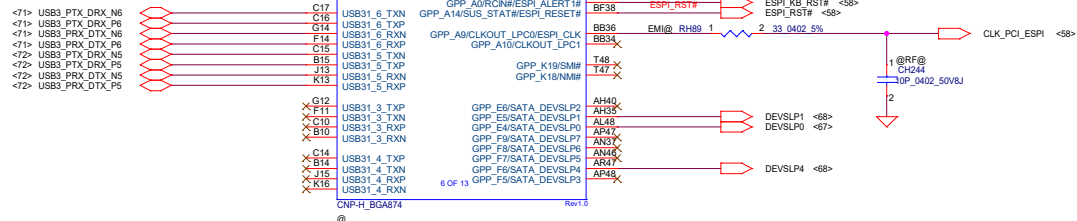
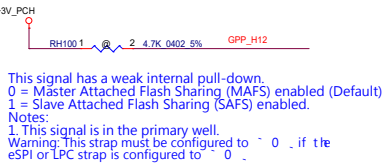
CFL_S62_IP_CRB_CFLS_LGA

Trace width / Spacing = 10 / 12 mils

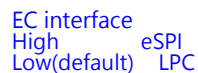
AB40 DDR_VREF_CA
AC40 DDR_VREF_DQ
AC39 DDR_VREF_DQ

Trace width / Spacing = 10 / 12 mils



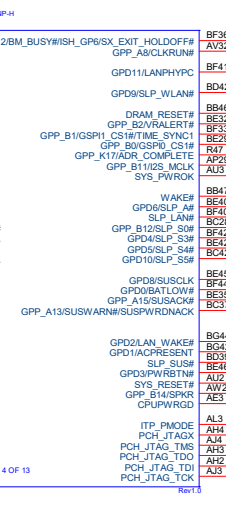


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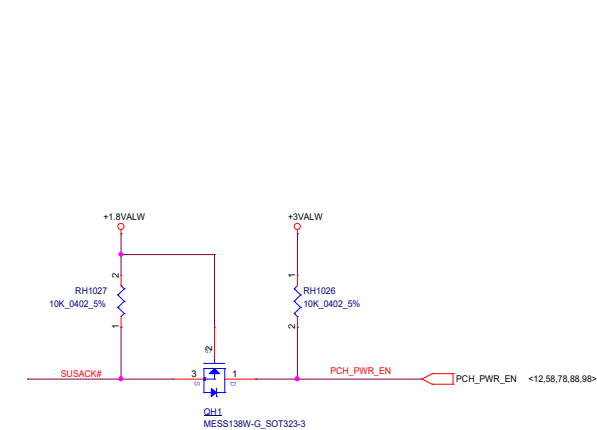
Notes:

1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.



This signal has an internal pull-down.
 0 = Disable IntelR DCI-OOB (Default)
 1 = Enable IntelR DCI-OOB

1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.



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				PCH (2/7) PM,HDA,SMB,JTAG
				LA-G881P
			Issue	Compal January 18 2019
			Sheet	12 of 161

UH1
S IC A31 FHSSKU04 QNDQ A1 BGA 874P PCH-H
SA0000B40L
CPCHE5@

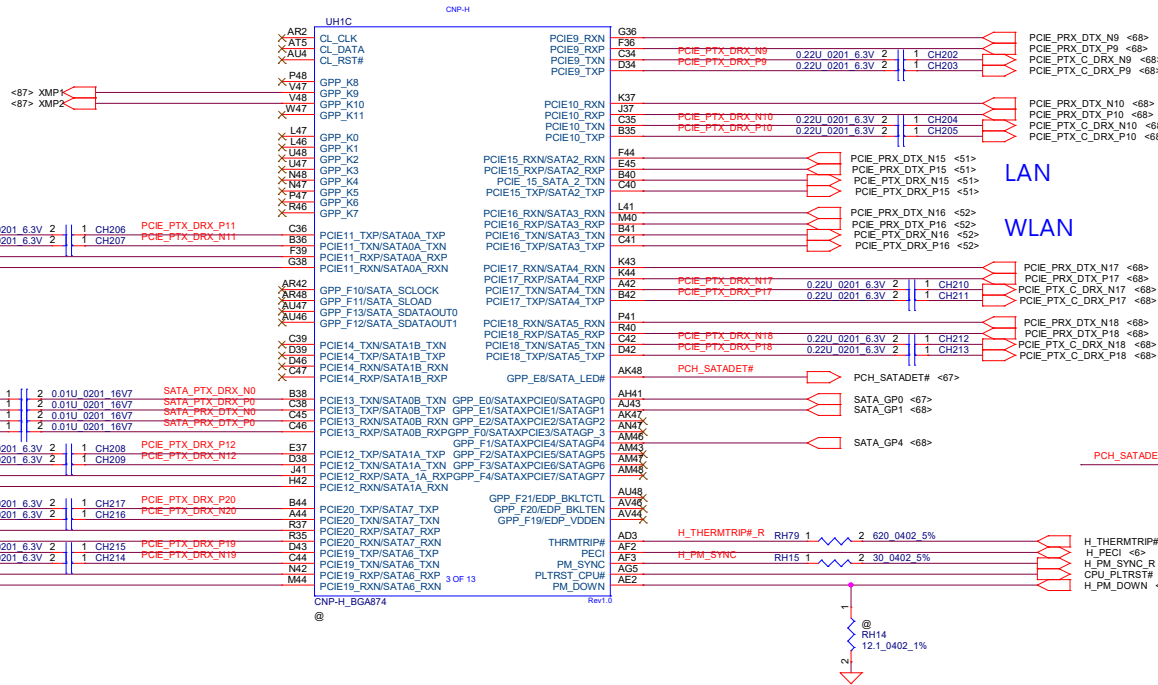
UH1
S IC A31 FHZ390 QQLP B0 BGA 874P PCH-H
SA0000C500L
CPCHE5@

M.2 SSD Slot#2
PCIe/SATA

SATA HDD

M.2 SSD Slot#2
PCIe/SATA

M.2 SSD Slot#1
PCIe/SATA

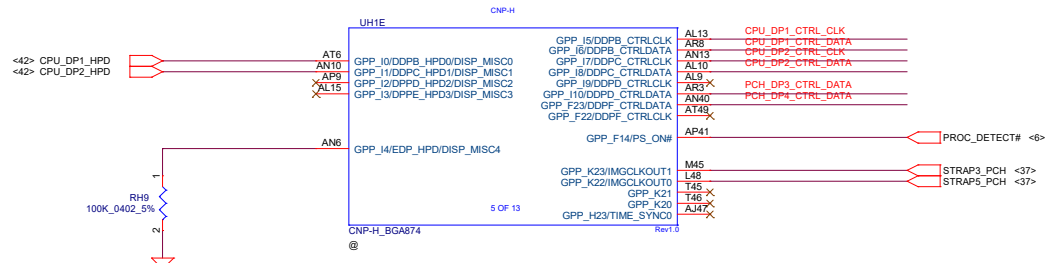


M.2 SSD Slot#1
PCIe/SATA

LAN

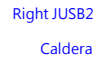
WLAN

M.2 SSD Slot#1
PCIe/SATA

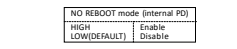
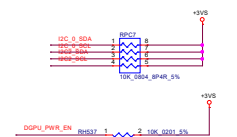
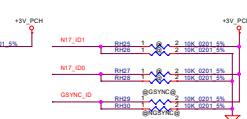
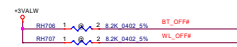


DDP[B.F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B~D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.

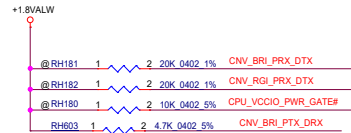
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/03/29	Deciphered Date	2019/03/29	Title	PCH (3/7) SATA,DDC,PCIe
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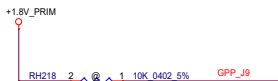


575179_Intel_Pulsar_CNVi_Schematic_Checklist_Rev3.1



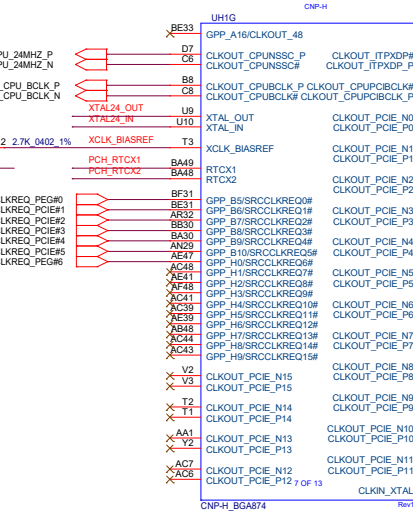
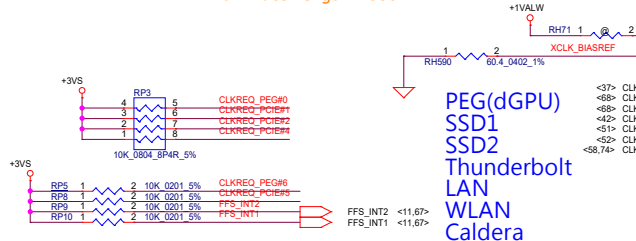
An external pull-high or pull-down is required
 0 = Integrated CNVi enable
 1 = Integrated CNVi disable

<S2> CNV_BR1_PTX_DRX_R
 <S2> CNV_BR1_PTX_DTX
 <S2> CNV_RGI_PTX_DRX_R
 <S2> CNV_RGI_PTX_DTX

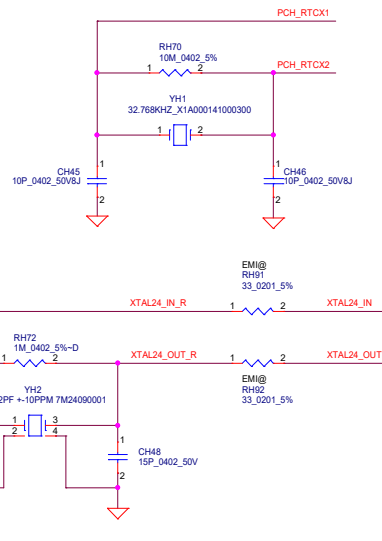


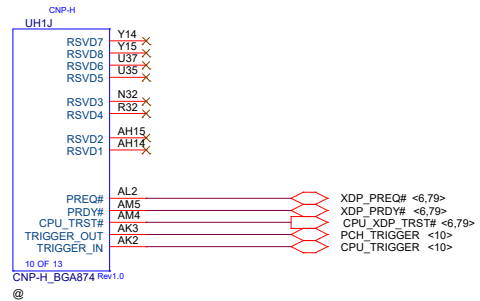
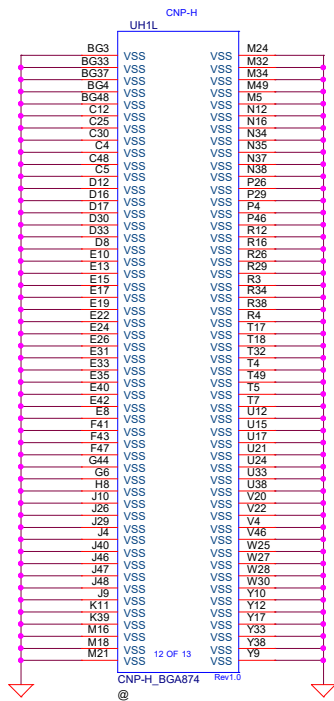
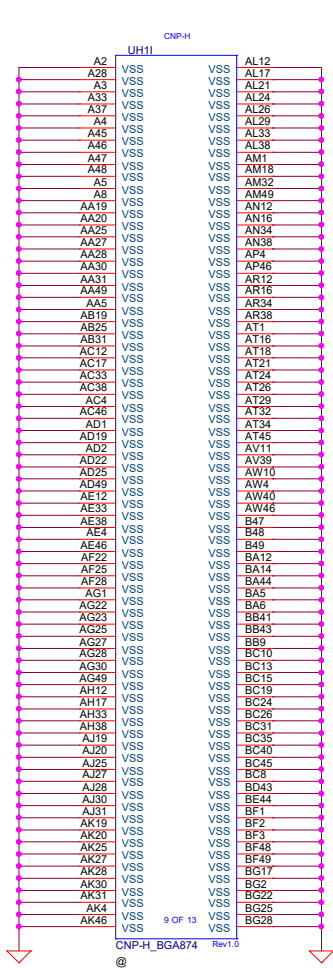
The signal has a weak internal pull-down
 0 = VCCPSPI is connected to 3.3V rail
 1 = VCCPSPI is connected to 1.8V rail
 Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a 1 for the proper functionality of the SPI (Flash) I/Os

Net : XCLK_BIASREF
 Trace Width/Space: 15mil /15 mil
 Max Trace Length: 1000 mil



#571483_CFL_H_RVP_CRB_TDK_Rev0p7
 Recommend external test point





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				PCH (7/7) GND				
				Size	Document Number		Rev	
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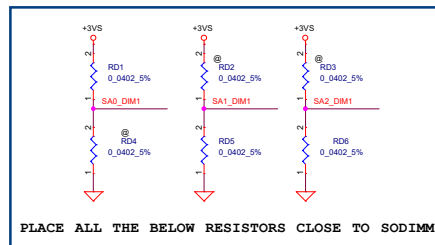
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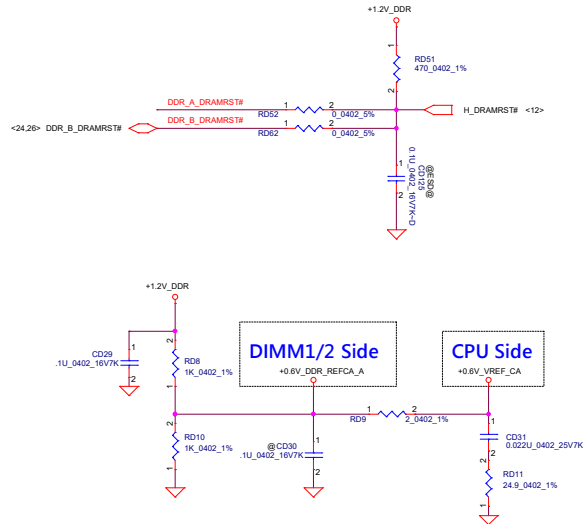
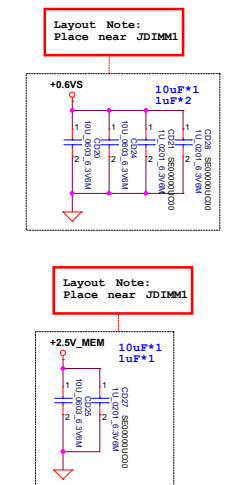
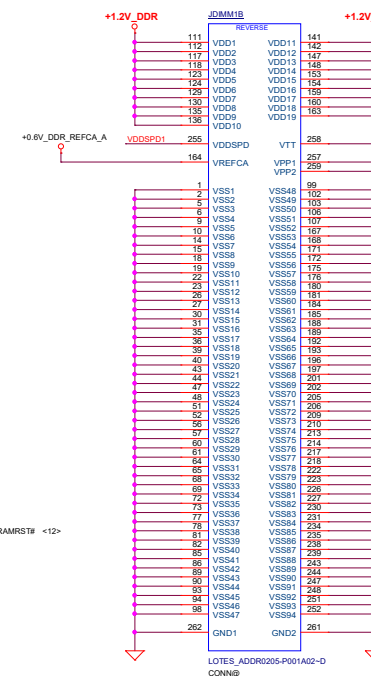
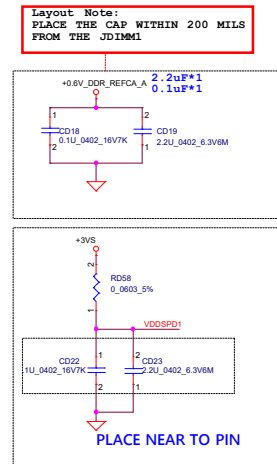
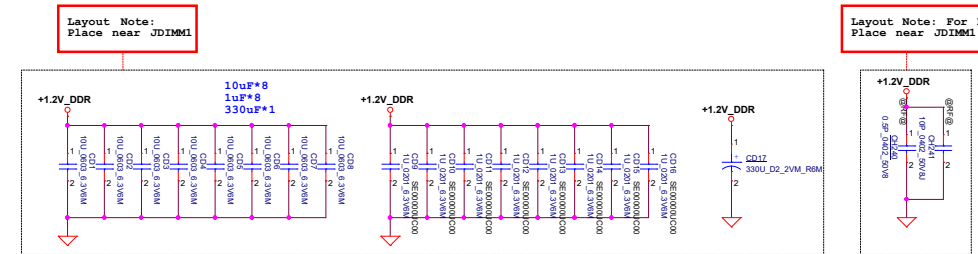
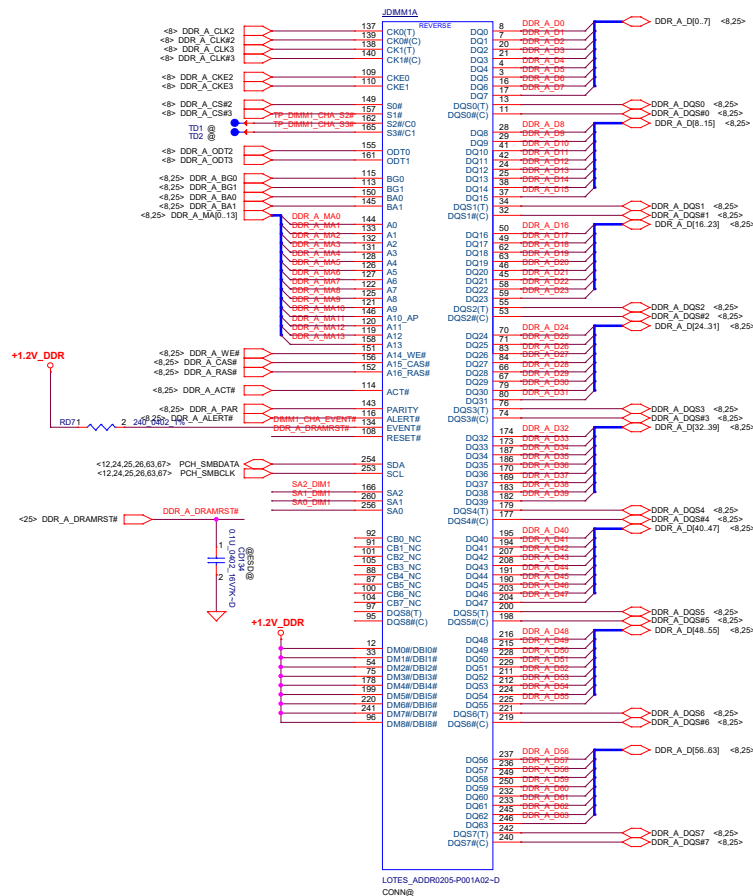
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Interleaved JDIMM1



	SA0	SA1	SA2
DIMM1	1	0	0
DIMM2	0	0	0
DIMM3	1	1	0
DIMM4	0	1	0

(4.0 mm) STD



The figure shows three identical circuit diagrams side-by-side, each representing a different channel of a sensor array. Each diagram consists of a vertical chain of components connected between a +3V5 supply and ground.

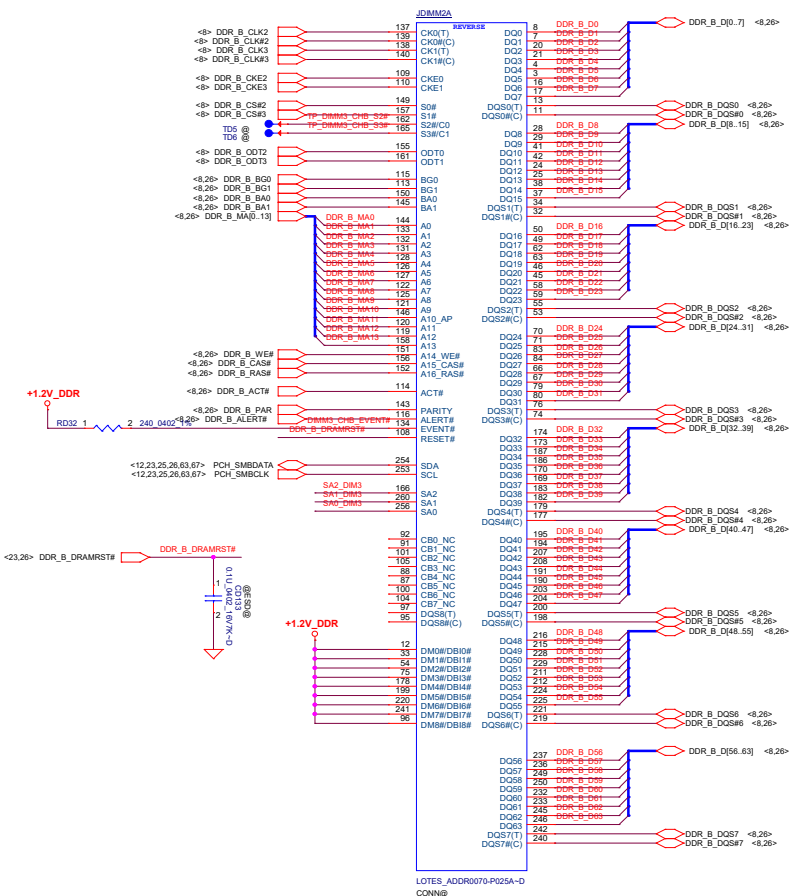
- Channel 1 (Left):** The top component is a resistor labeled RD26 with a value of 0_0402_5%. Below it is a red horizontal line representing a signal line labeled SA0_DIM3. The bottom component is a resistor labeled RD29 with a value of 0_0402_5%, connected to ground.
- Channel 2 (Middle):** The top component is a resistor labeled RD27 with a value of 0_0402_5%. Below it is a red horizontal line representing a signal line labeled SA1_DIM3. The bottom component is a resistor labeled RD30 with a value of 0_0402_5%, connected to ground.
- Channel 3 (Right):** The top component is a resistor labeled RD28 with a value of 0_0402_5%. Below it is a red horizontal line representing a signal line labeled SA2_DIM3. The bottom component is a resistor labeled RD31 with a value of 0_0402_5%, connected to ground.

In all three diagrams, the resistors are represented by blue zigzag lines, and the ground connection is shown as a triangle with a horizontal line.

	SA0	SA1	SA2
DIMM1	1	0	0
DIMM2	0	0	0
DIMM3	1	1	0
DIMM4	0	1	0

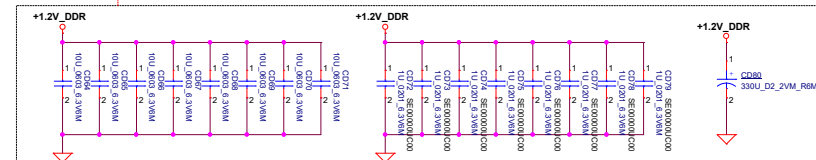
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

(8.0 mm) RVS

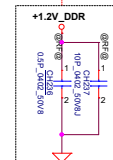


Layout Note:
Place near JDIMM3

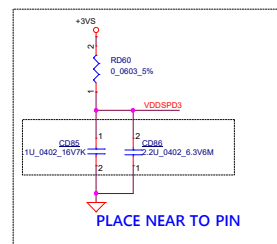
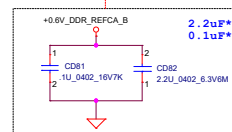
10uF*8
1uF*8
330uF*1



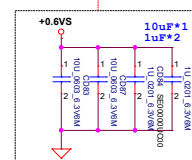
Layout Note: For
Place near JDIMM3



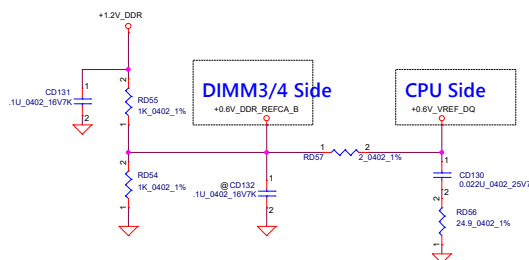
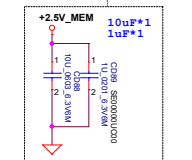
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM3



Layout Note:
Place near JDIMM3



Layout Note:
Place near JDIMA



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Date:	Tuesday, January 18, 2018	Sheet	24	of	101

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RD14
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RD15
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RD16
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RD17
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PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

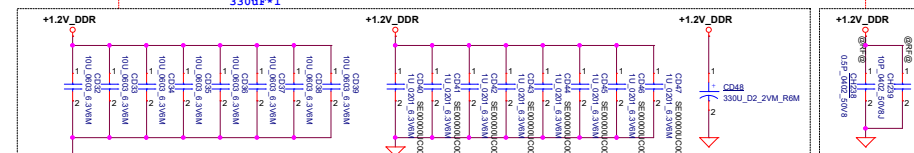
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DIMM2	0	0	0
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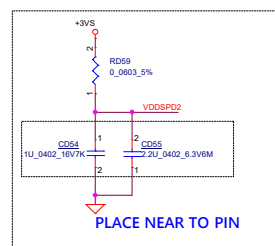
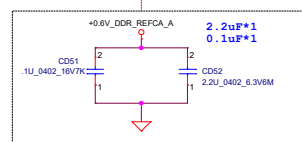
Layout Note:
Place near JDIMM2

10uF*8
1uF*8
330uF*1

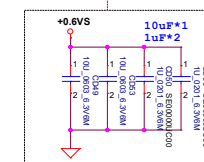
Layout Note: For RF
Place near JDIMM2



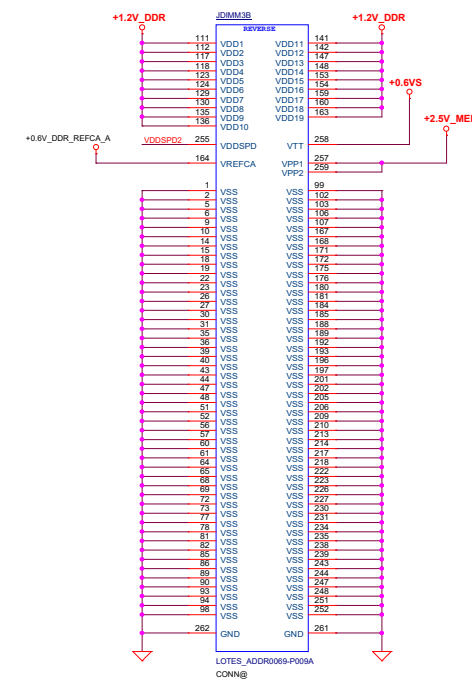
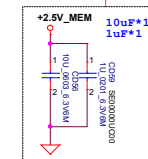
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2



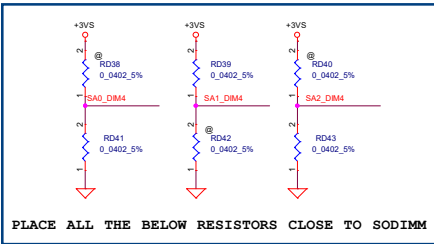
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM

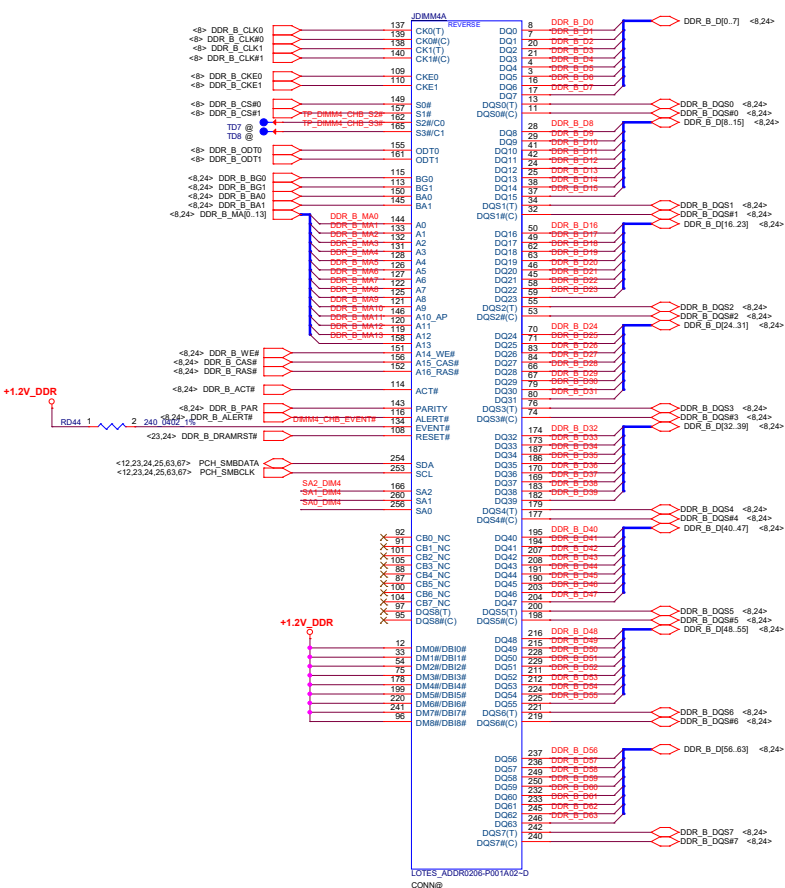
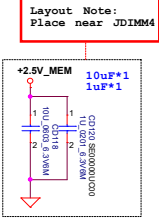
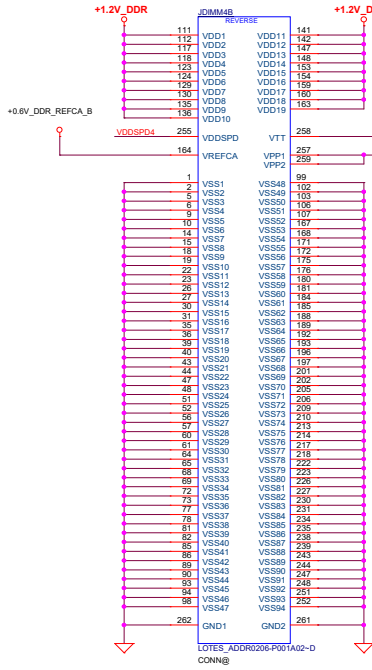
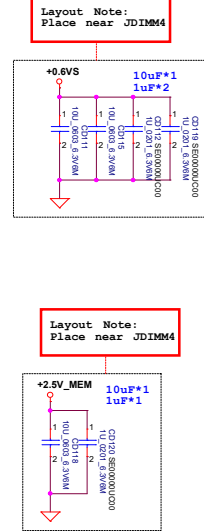
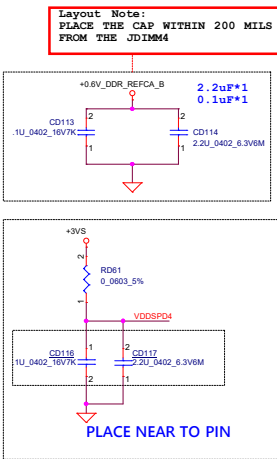
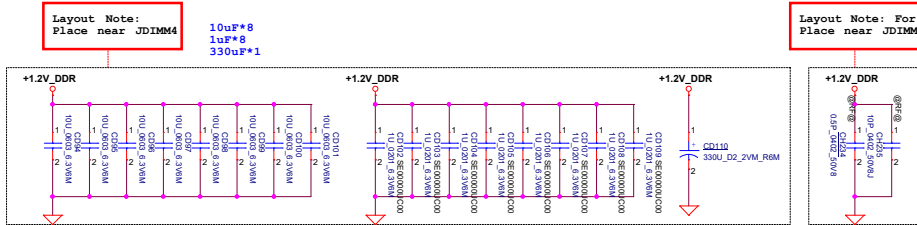


Interleaved JDIMM4



	SA0	SA1	SA2
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DIMM2	0	0	0
DIMM3	1	1	0
DIMM4	0	1	0

(4.0 mm) RVS



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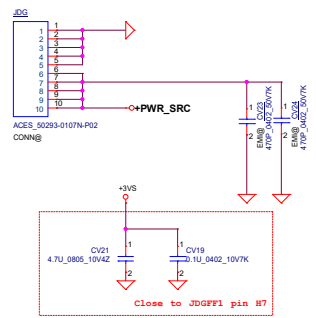
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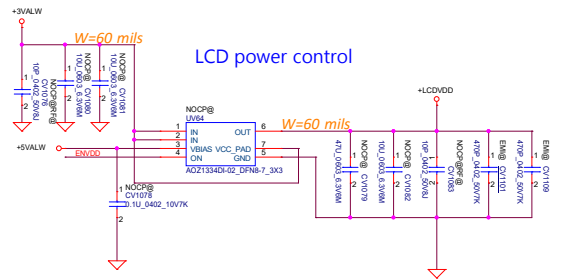
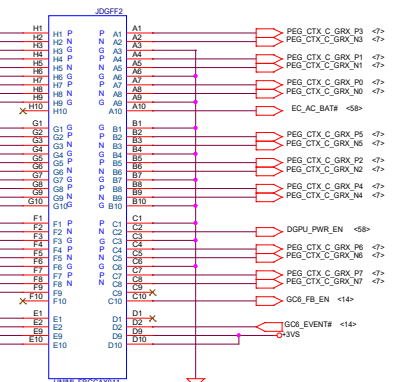
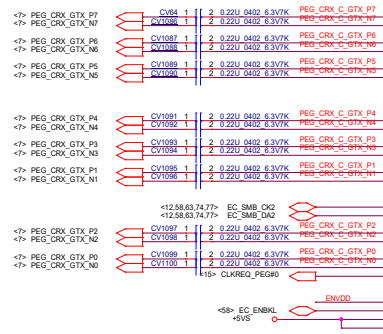
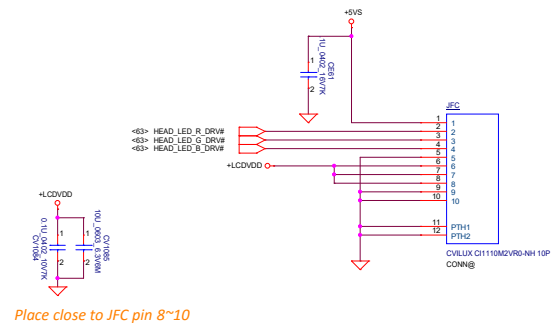
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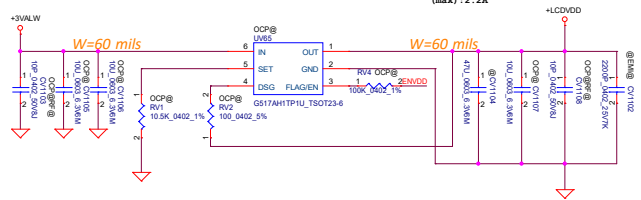
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X-Beam I/per pin=0.5A
I/per connector=0.75A



Vout=3.3V
Imax=1.33A
OCP(min):1.8A
(typ):2A
(max):2.2A



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CONN@
CLIP.10P2X7P2_SHIELDING_CASE1
EQ0X000000

PCIE TX

PCIE CLK

CPU DDI1

CPU DDI2

CPU_DP1_AUXN_C RT76 1 2 100K 0201 5%
CPU_DP2_AUXN_C RT77 1 2 100K 0201 5%
CPU_DP1_AUXP_C RT78 1 2 100K 0201 5%
CPU_DP2_AUXP_C RT79 1 2 100K 0201 5%

+3VALW_TBT
TBT_TDI
TBT_TMS
TBT_TCK
TBT_TDO

TBTA_LSTX RT21 2 1 10K 0201 5%
CLKREQ_PCIE#_R RT20 2 1 10K 0201 5%
TBT_RTD3_RST# RT6952 @RTD3@ 10K 0201 5%
TBT_RST#_R RT7232 @RTD3@ 10K 0201 5%

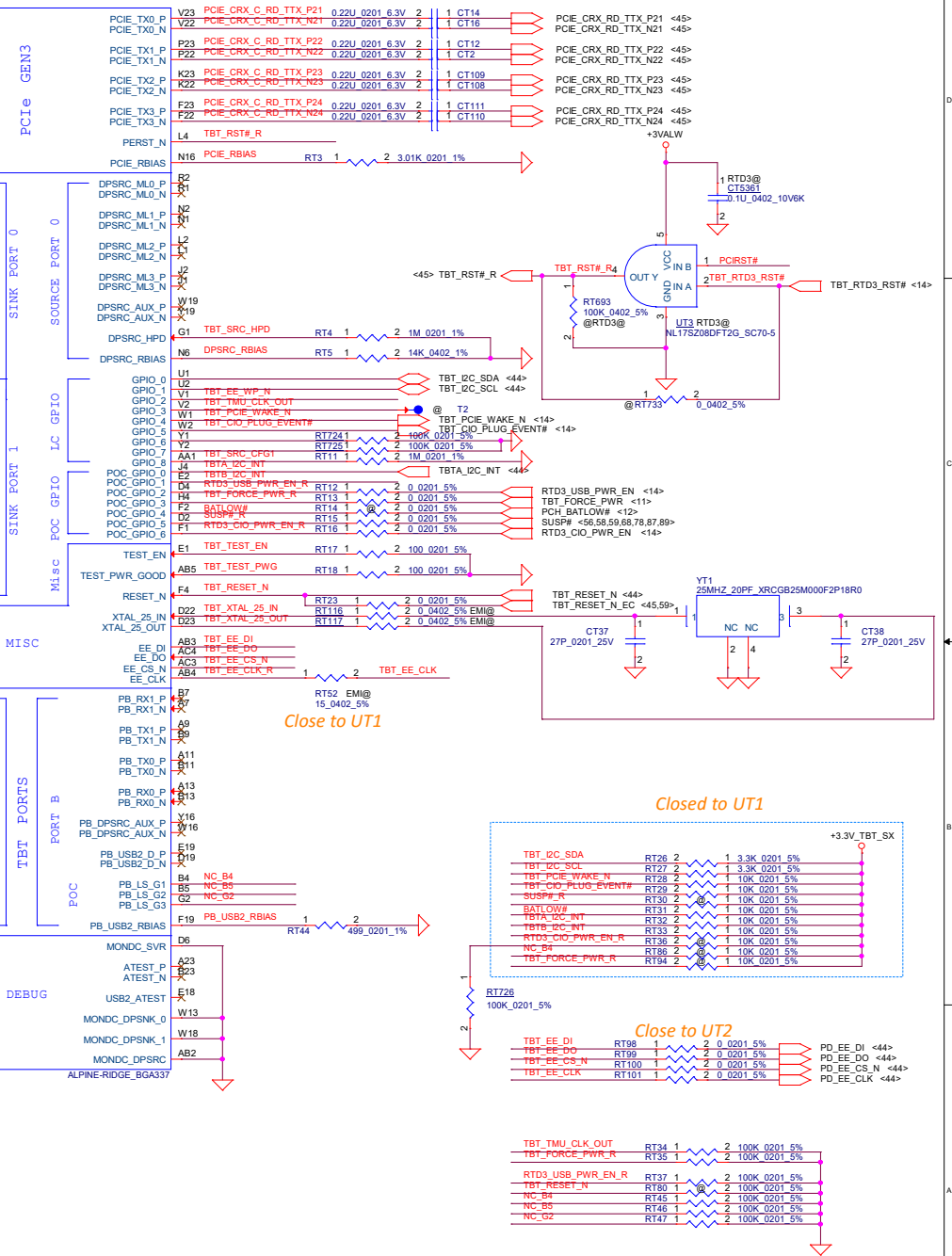
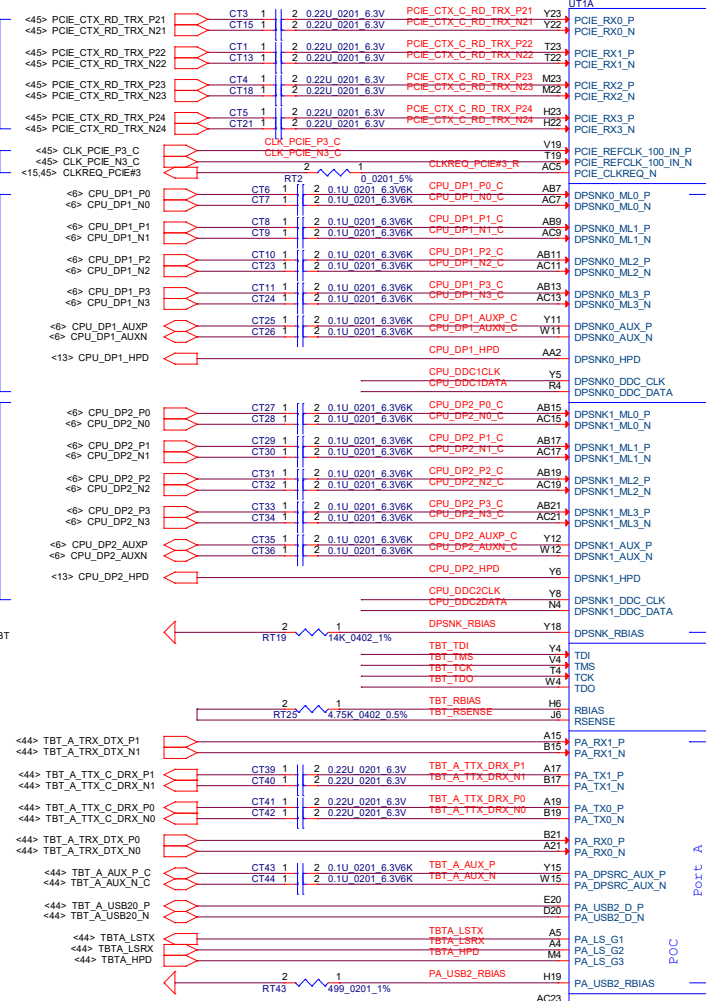
CPU_DDC1CLK RT1271 2 100K 0201 5%
CPU_DDC1DATA RT1261 2 100K 0201 5%
CPU_DDC2CLK RT1281 2 100K 0201 5%
CPU_DDC2DATA RT1281 2 100K 0201 5%

CPU_DP1_HPD RT38 1 2 100K 0201 5%
CPU_DP2_HPD RT39 1 2 100K 0201 5%
TBTA_LSTX RT40 2 1 1M 0201 1%
TBTA_LSRX RT42 2 1 1M 0201 1%

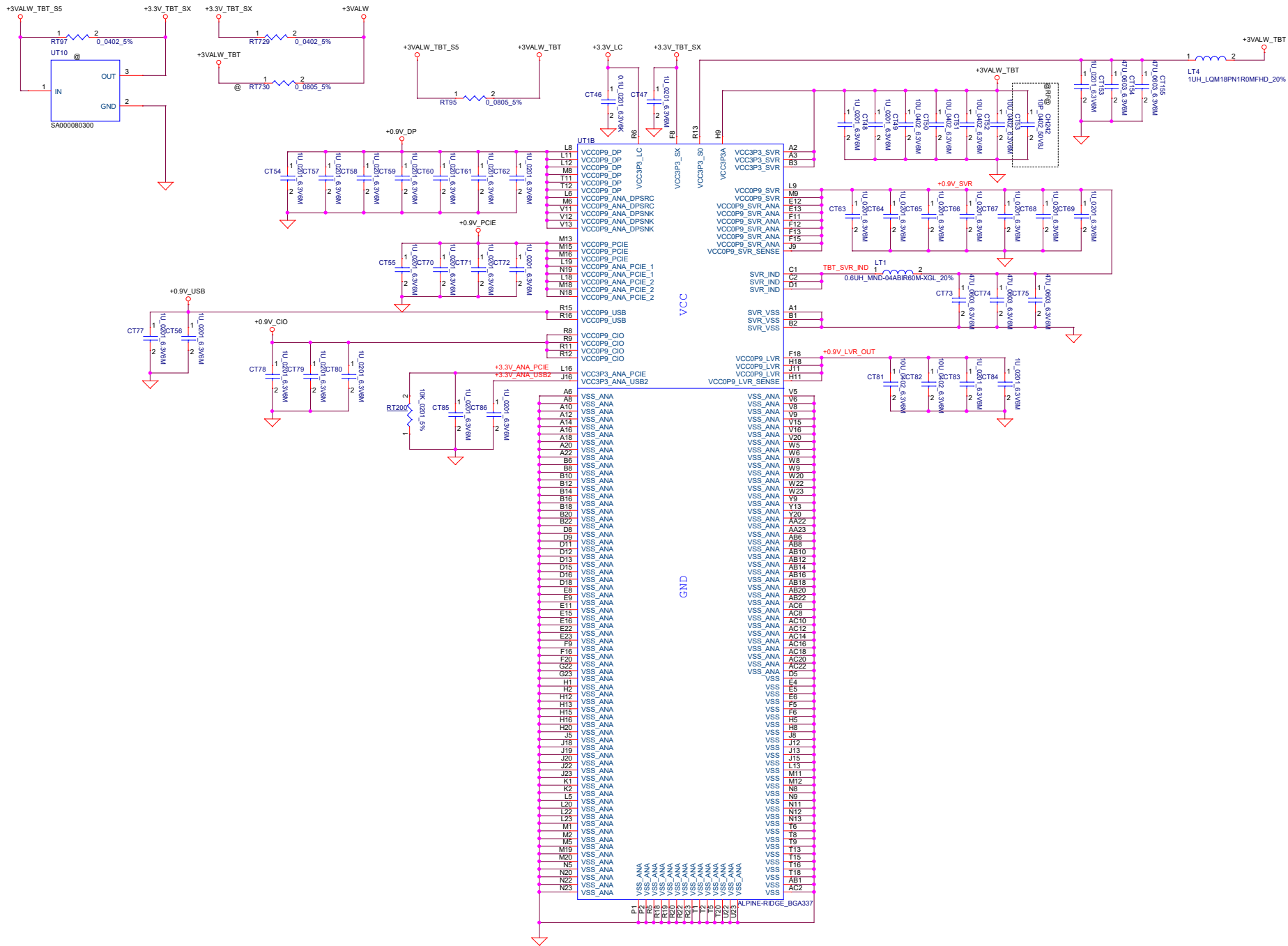
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+3.3V_FLASH
RT50 1 2 2.2K 0201 5%
RT49 1 2 2.2K 0201 5%
RT48 1 2 3.3K 0201 5%
TBT_EE_CS_N
TBT_EE_DO
TBT_EE_WP_N
TBT_EE_DI
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RT51 3.3K_0201_5%
RT122 33_0402_5%
RT156 22P_0402_50V8J-D

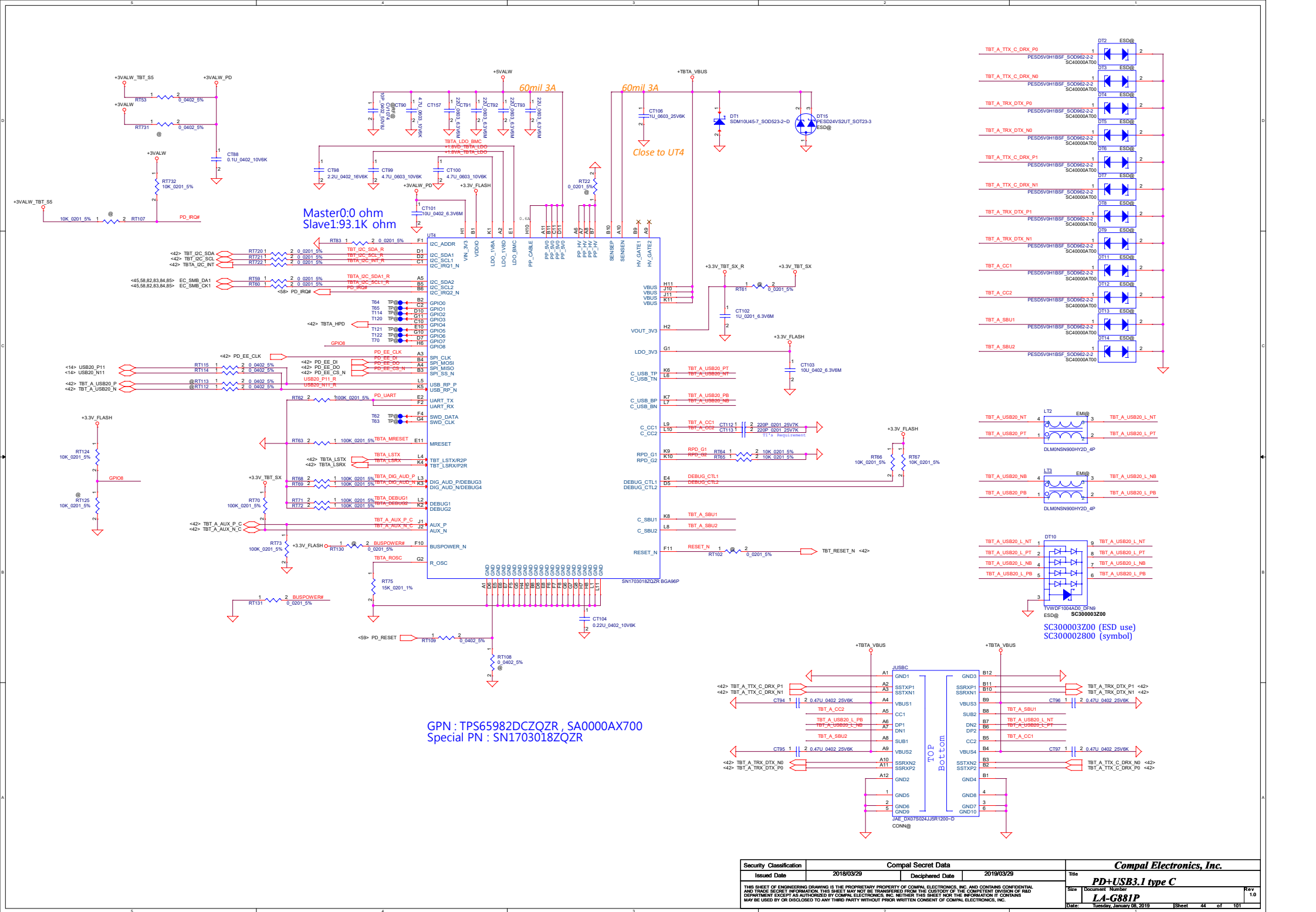
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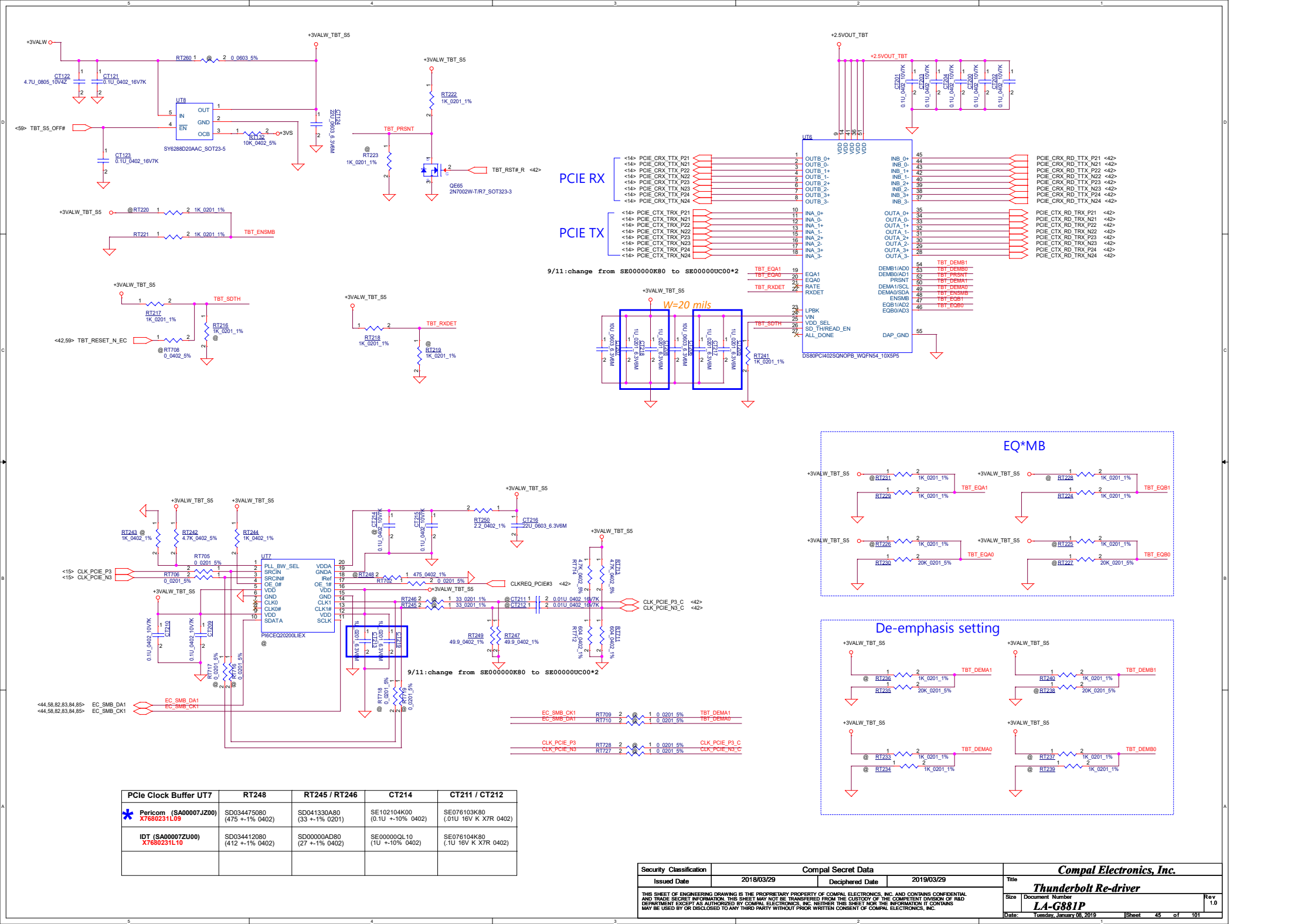


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				Date:	Tuesday, January 08, 2019	Sheet 47 of 101

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				Size	Document Number	Rev
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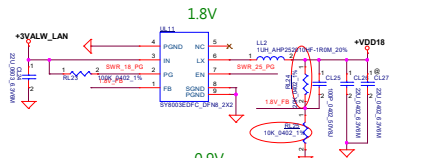
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				Date:	Tuesday, January 08, 2019
				Sheet	50 of 101
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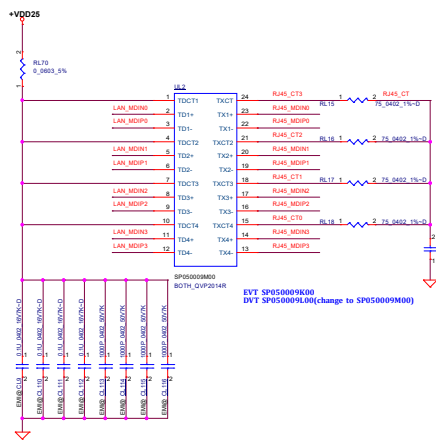
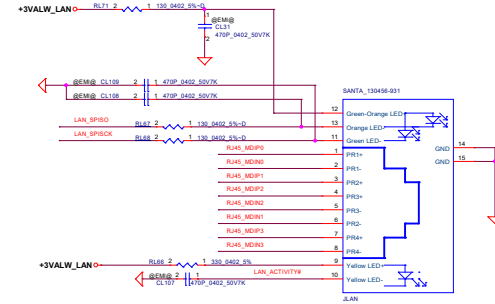
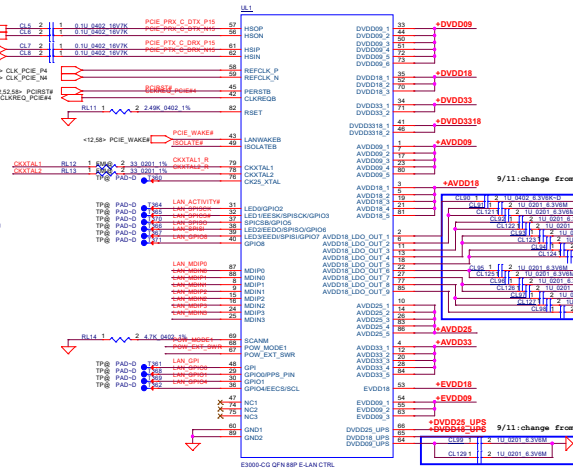
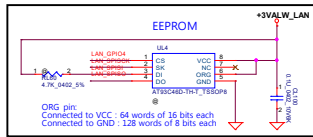
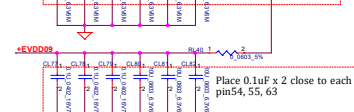
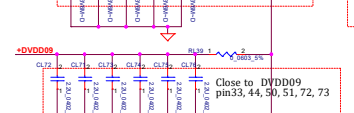
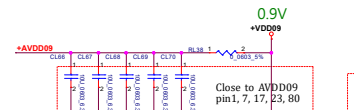
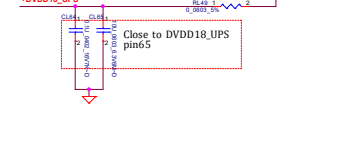
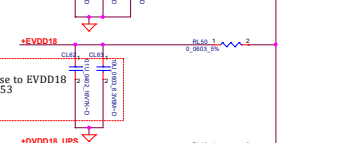
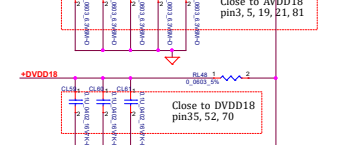
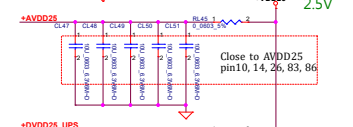
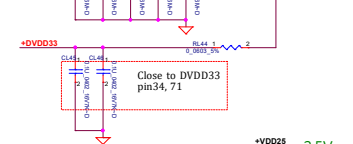
LL4 need close to rUL13.6 and placement the same layer



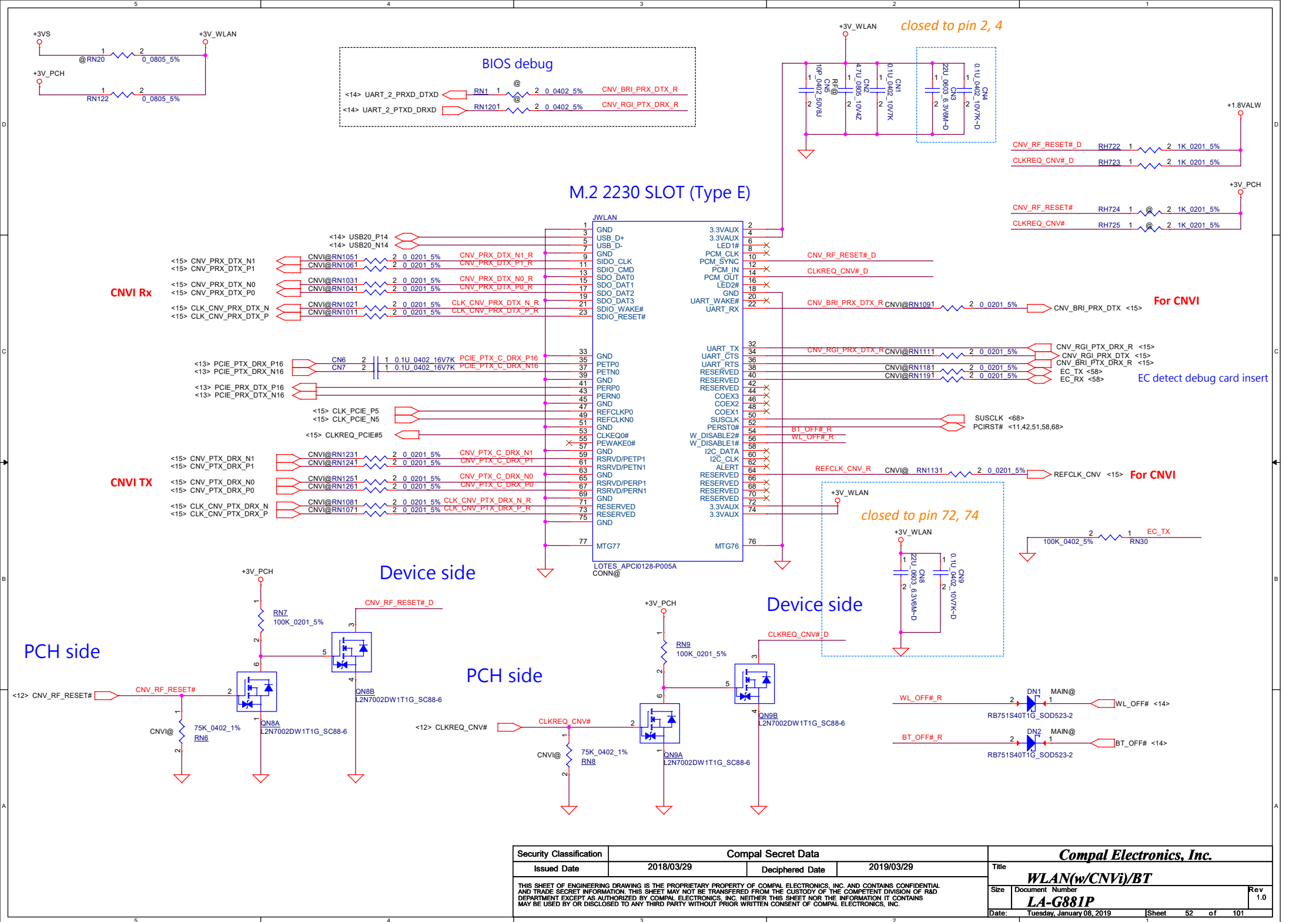
+AVDD33

+3VALW_LAN 3.3V

2 10uF close to AVDD33 pin 4, 12, 20, 28, 84



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				Size	Document Number	Rev	
					LA-G881P	1.0	
				Date:	Tuesday, January 08, 2019	Sheet	53 of 101

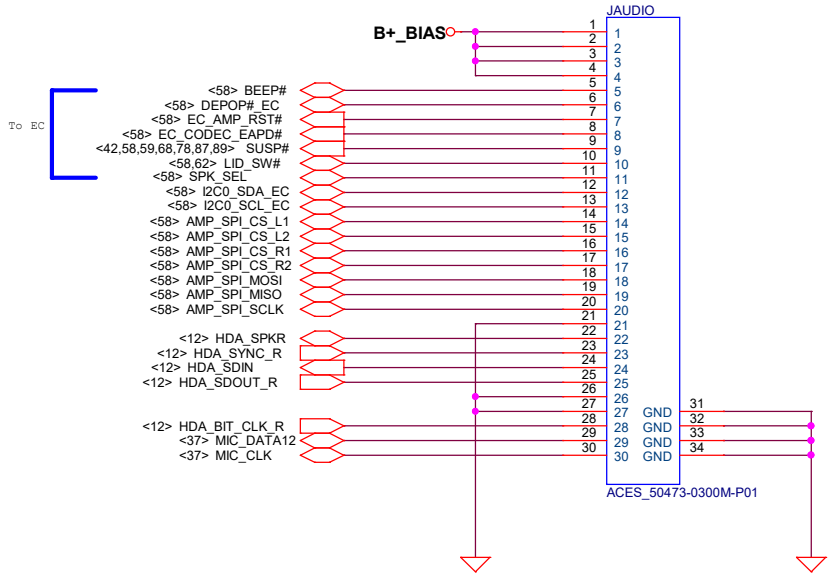
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				Date:	Tuesday, January 08, 2019
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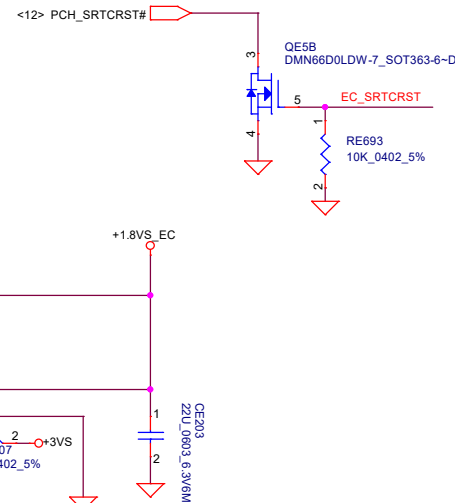
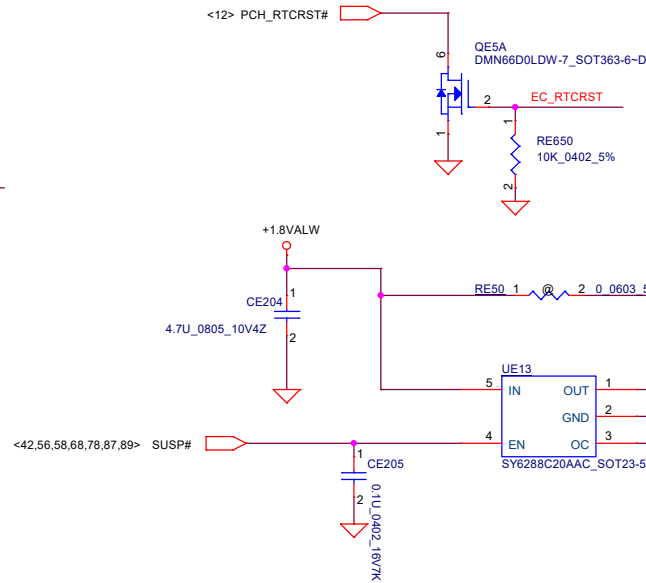
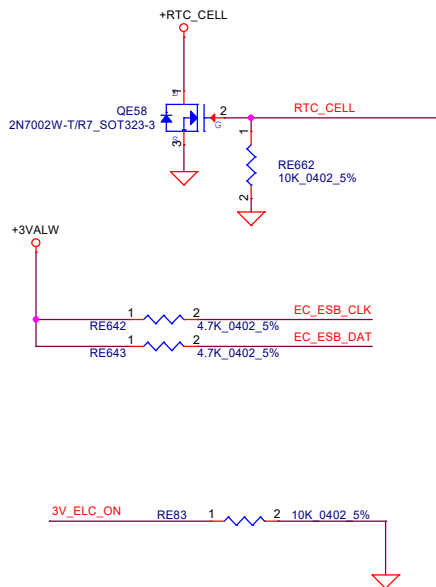
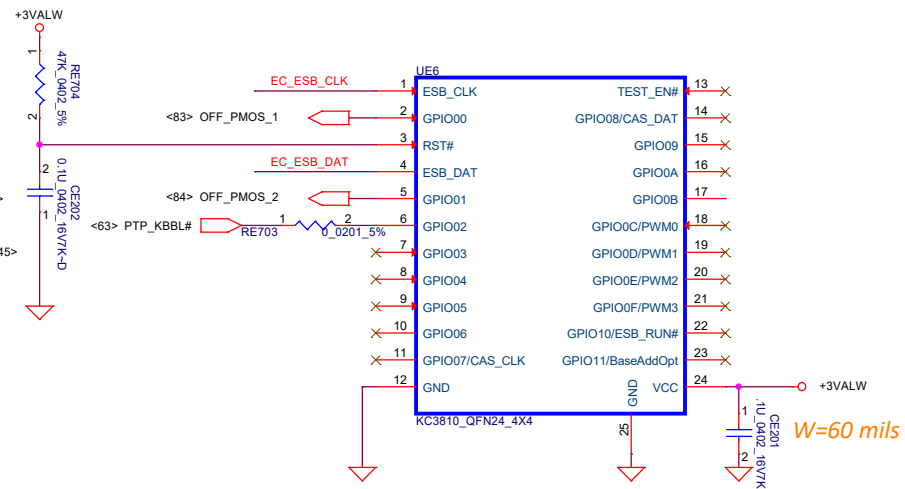
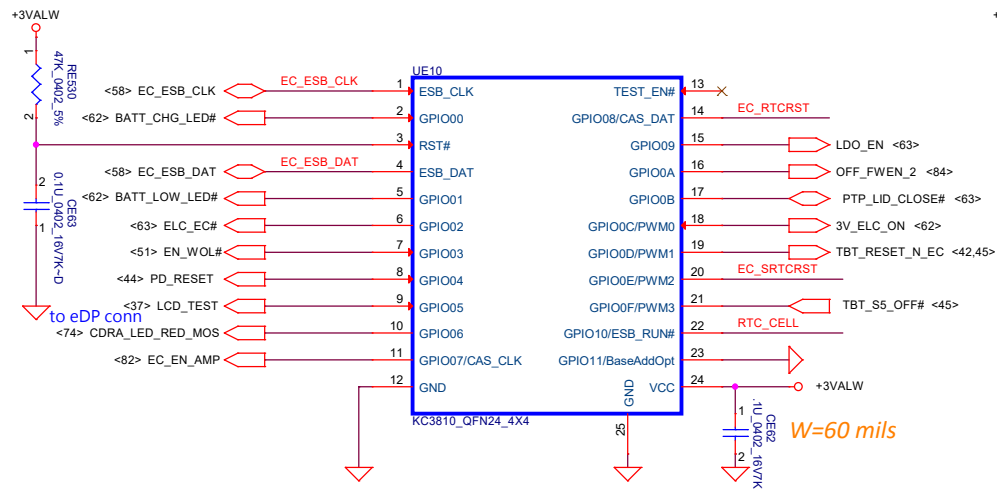
M/B to Audio/B



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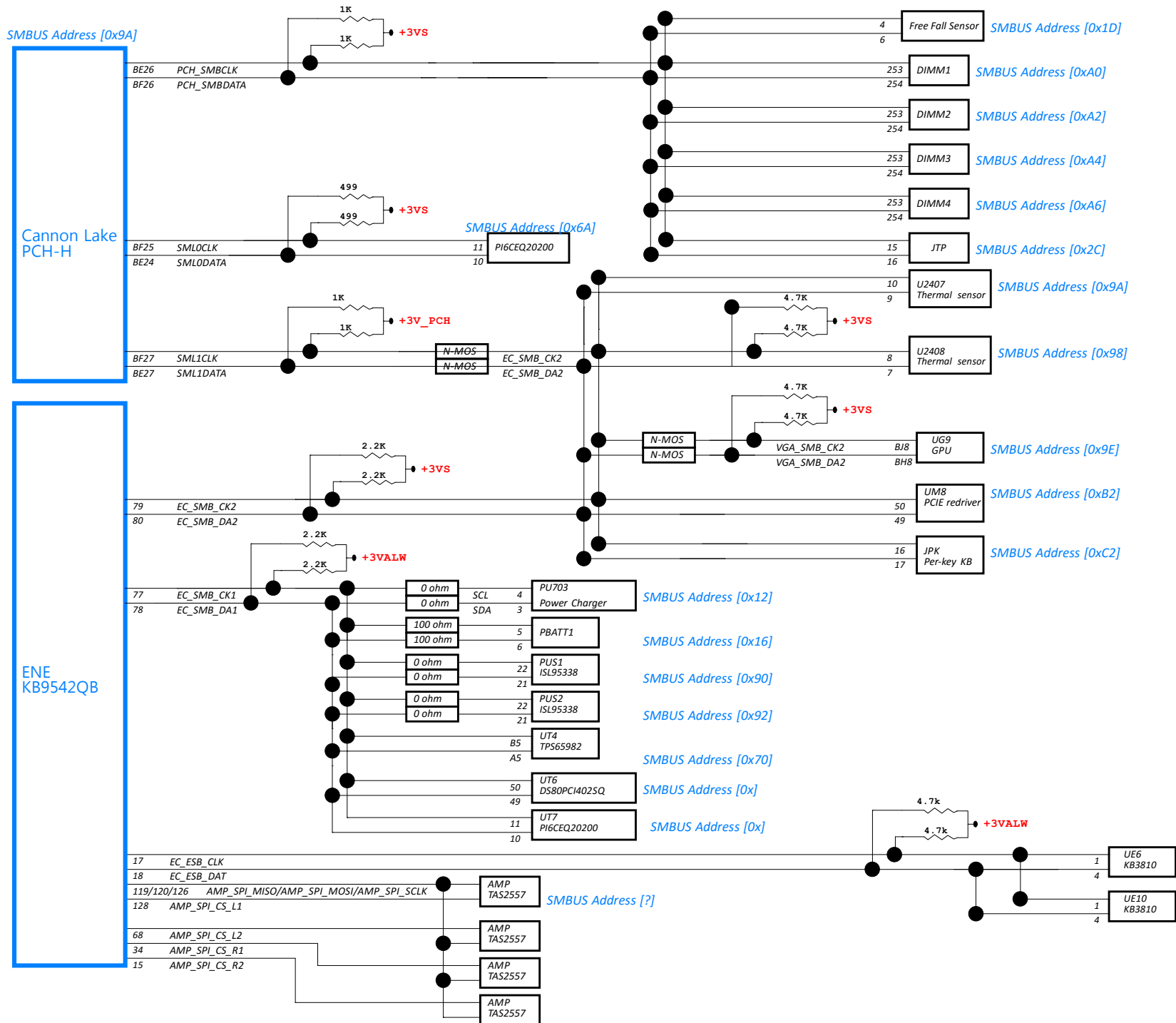
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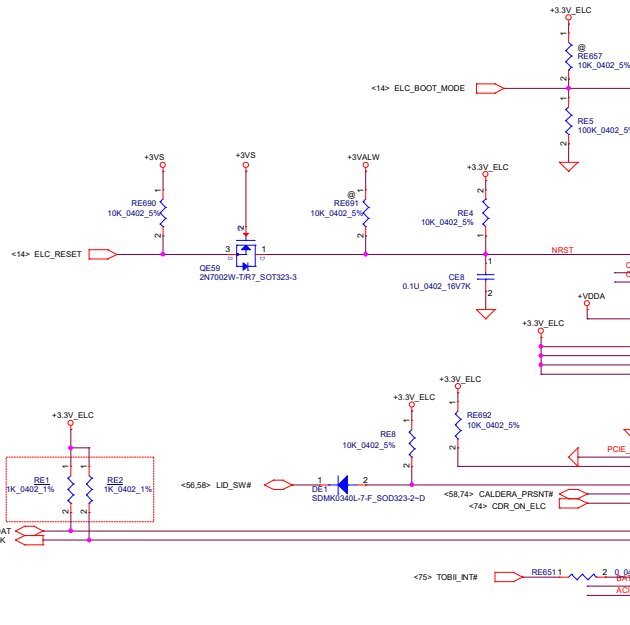
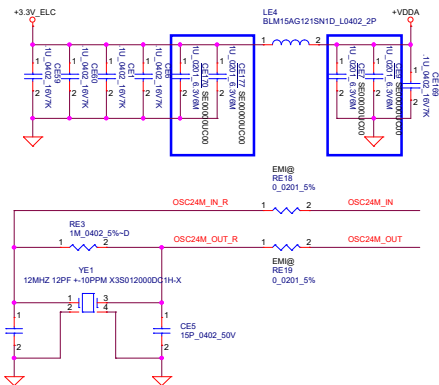
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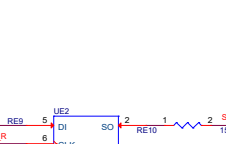
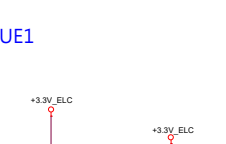
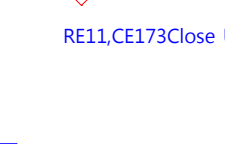
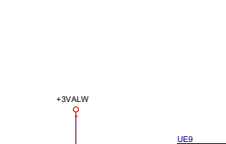
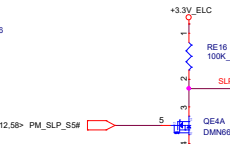
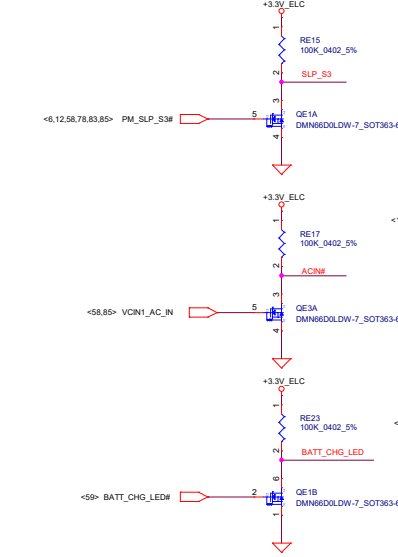
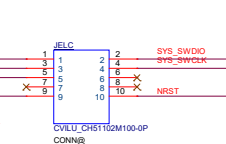
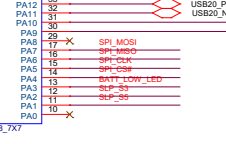
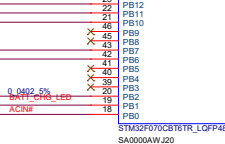
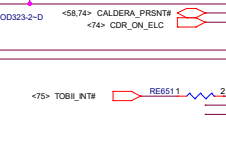
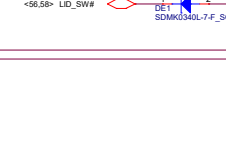
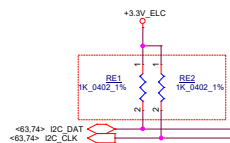
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9/11:change from SE000000K80 to SE000000C00*2



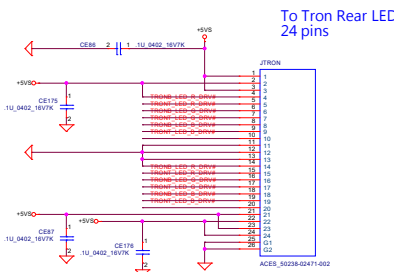
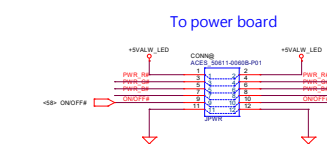
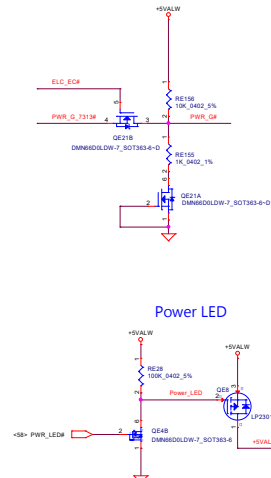
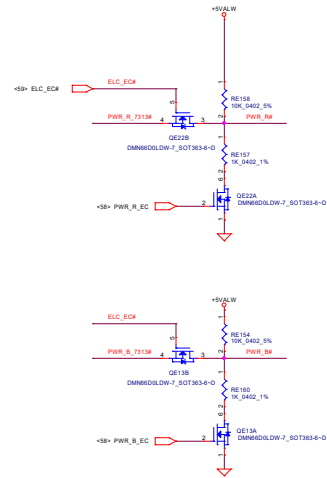
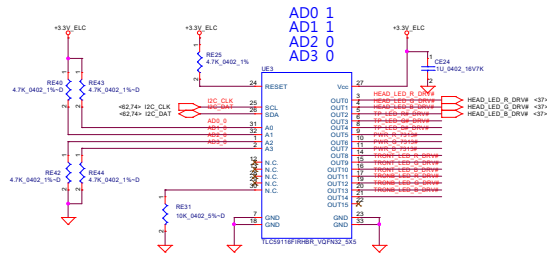
BOOT0 = 1 HW bootloader
BOOT0 = 0 SW bootloader



+3.3V_ELC behavior

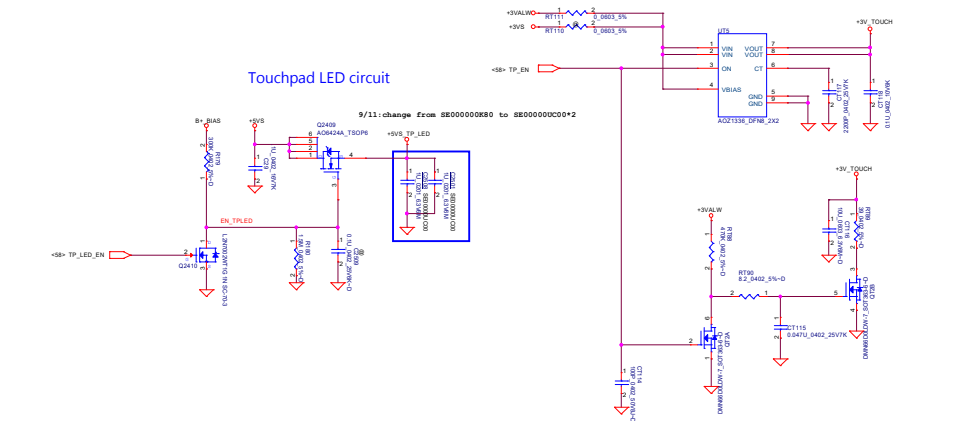
	S0	S3	S4	S5
AC IN (battery low)	ON	ON	ON	ON
AC IN (battery full)	ON	ON	OFF	OFF
BATT only	ON	ON	OFF	OFF

Update PWR BTN LED behavior when AC IN (battery full) at S4



NOTE:
CE86 close to JTRON PIN1 and PIN3
CE175 close to JTRON PIN2 and PIN4
CE87 close to JTRON PIN21 and PIN23
CE176 close to JTRON PIN22 and PIN24

Touchpad LED circuit



Per Key pin define

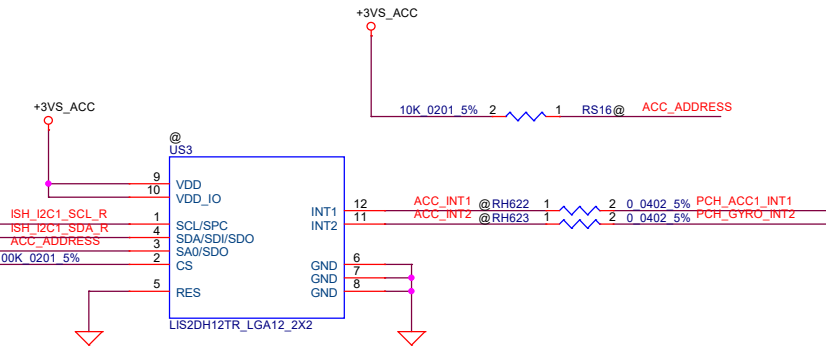
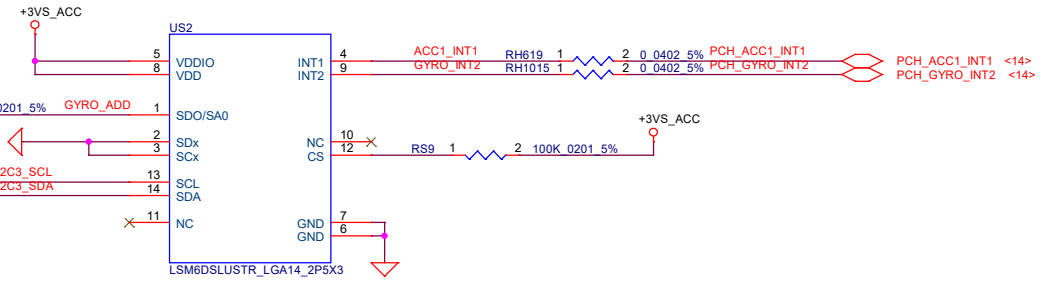
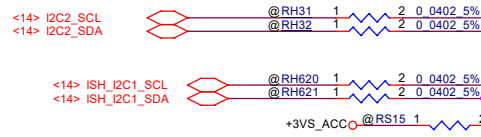
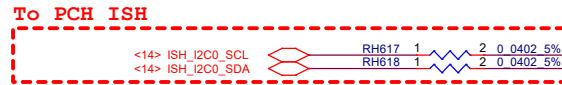
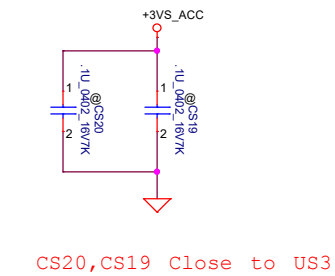
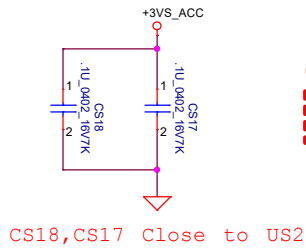
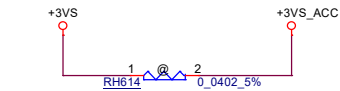
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- Pin6 NC
- Pin7~9 GND
- Pin10 D+
- Pin11 D-
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- Pin15 I2C_INT
- Pin16 I2C_CLK
- Pin17 I2C_DAT
- Pin18 LDO_EN
- Pin19~20 NC

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L1-G881P				Rev	1.0

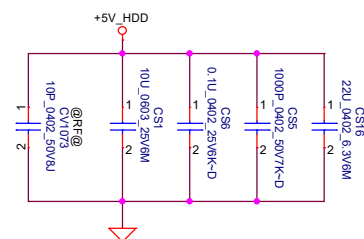
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				Date:	Tuesday, January 08, 2019
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				Rev	1.0
				LA-G881P	

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Issued Date	2018/03/29	Declassified Date	2018/03/29	Yes
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Size	A4			1/4
File	LA-G581P			1/4
Issue	Issued: January 28, 2019			1/4
Sheet	05			1/4



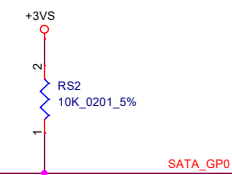
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/03/29	Deciphered Date	2019/03/29	Title	Reversed
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				Rev	1.0



D/SSD5

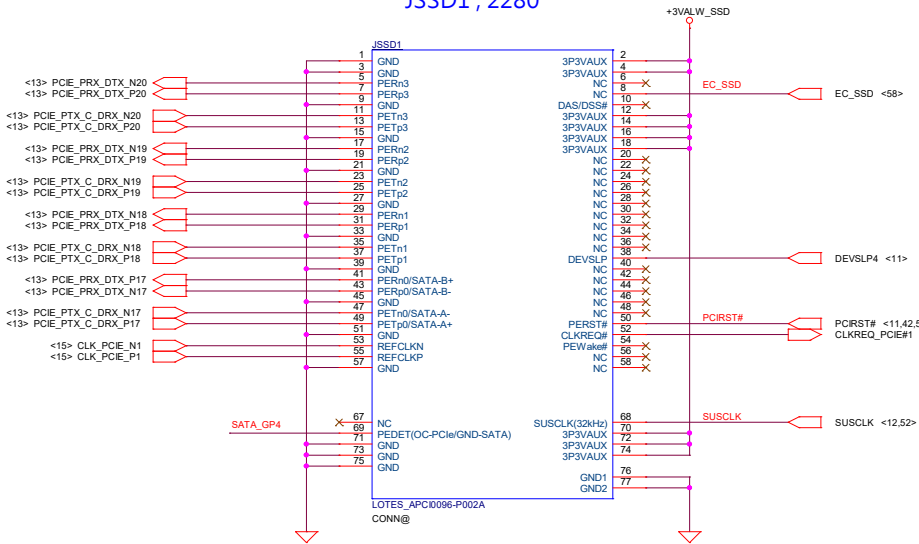
The diagram illustrates the electrical connection between a SATA controller and a JHDD (JetFlash HDD) device. On the left, the SATA controller pins are labeled: <13> SATA_PRX_C_DTX_N0, <13> SATA_PRX_C_DTX_P0, <13> SATA_PTX_C_DRX_N0, <13> SATA_PTX_C_DRX_P0, and <11> DEVSLP0. On the right, the JHDD pins are numbered 1 through 24, with additional labels G1, G2, G3, and G4 for pins 21-24. The connections are as follows: SATA_PRX_C_DTX_N0 to JHDD pin 1; SATA_PRX_C_DTX_P0 to JHDD pin 2; SATA_PTX_C_DRX_N0 to JHDD pin 4; SATA_PTX_C_DRX_P0 to JHDD pin 5; DEVSLP0 to JHDD pin 6; SATA_GP0 to JHDD pin 10; PCH_SATADET# to JHDD pin 11; FFS_INT2_CONN to JHDD pin 12; +5V_HDD to JHDD pin 18; and JHDD pin 17 to ground. A note 'ACES_50406-02071-001 CONN@' is located at the bottom right.

ACES_50406-02071-001
CONN@

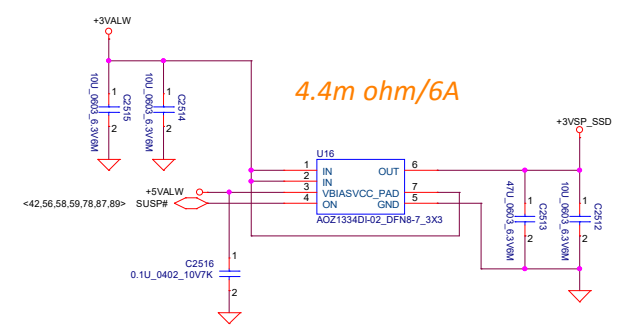
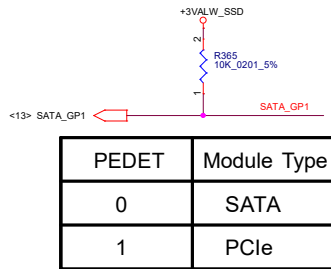
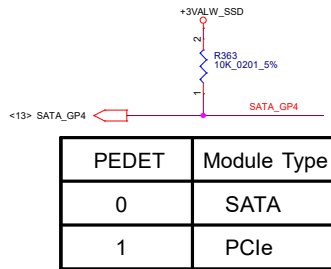
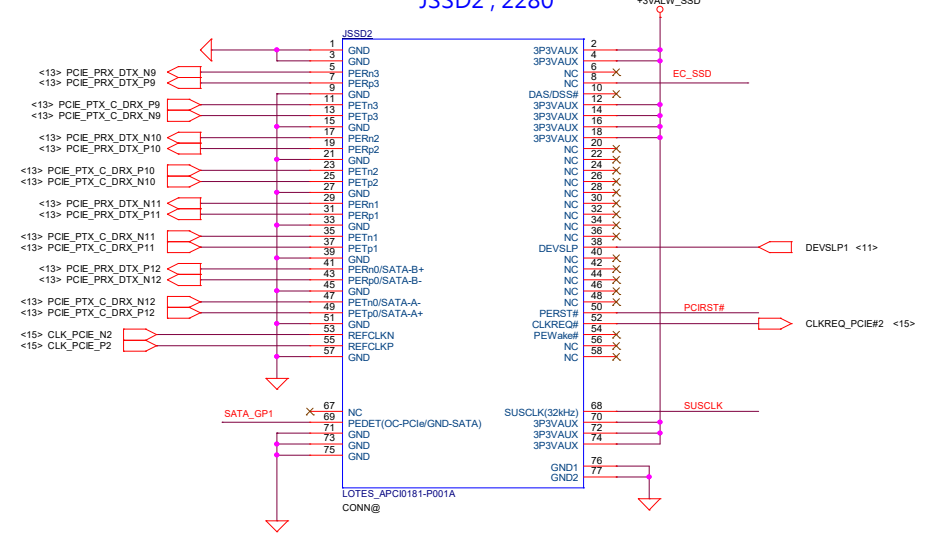
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Security Classification		Compal Secret Data		Compal Electronics, Inc. SATA HDD Connector	
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					Rev 1.0
Date: Tuesday, January 08, 2019				Sheet	67 of 101

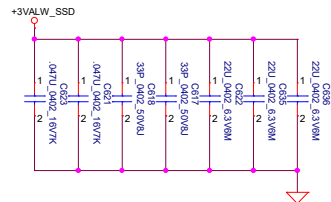
PCIe / SATA SSD JSSD1, 2280



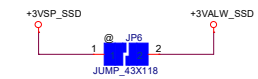
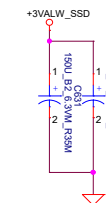
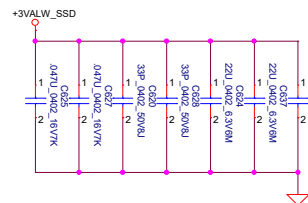
PCIe / SATA SSD JSSD2, 2280



JSSD1

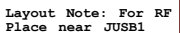


JSSD2

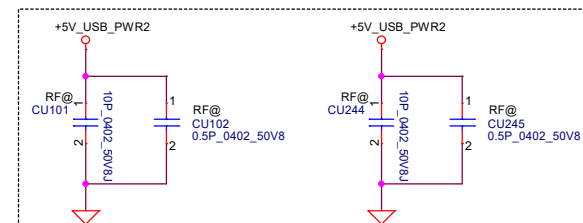
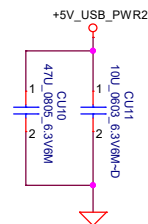
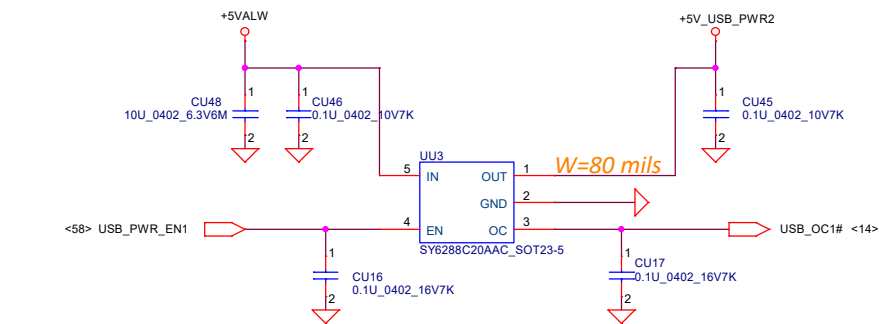


A	B	C	D	E

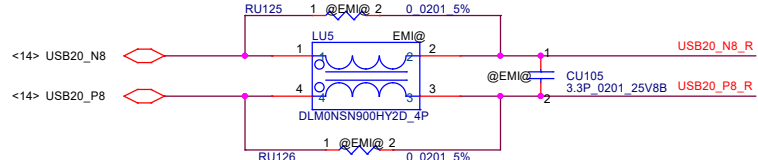
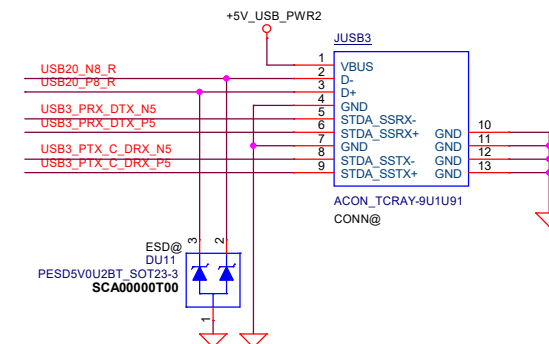
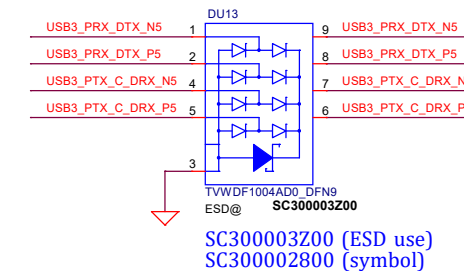
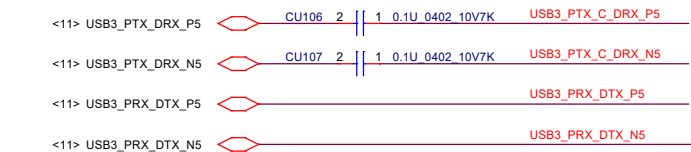
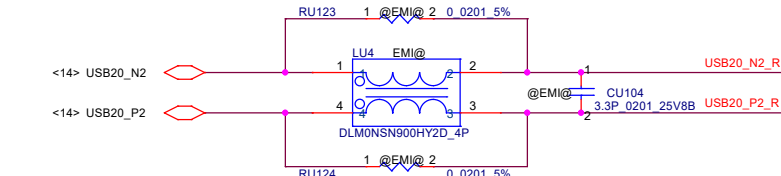
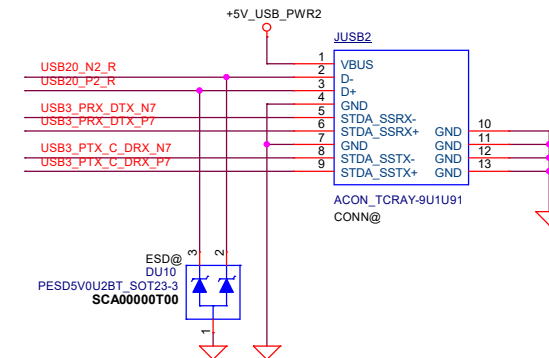
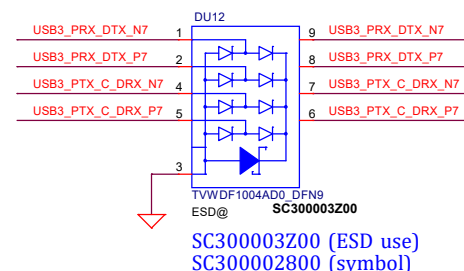
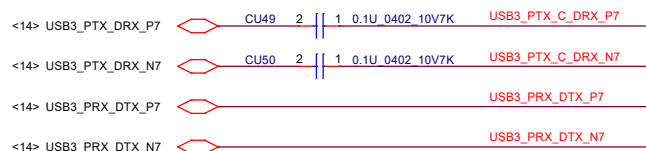
A	B	C	D	E



USB3_TEST
LFPS swing adjust. 3.3V tolerant.
Internally pulled down 150KΩ .
L: Normal LFPS swing (default)
H: Tune down LFPS swing

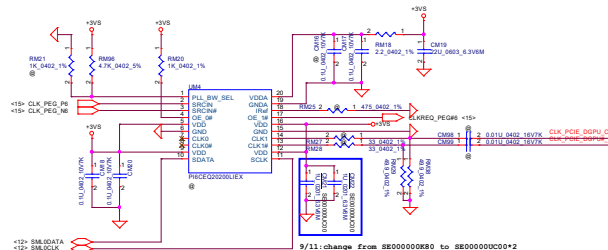


Layout Note: For RF
Place near JUSB2 JUSB3

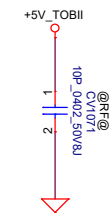
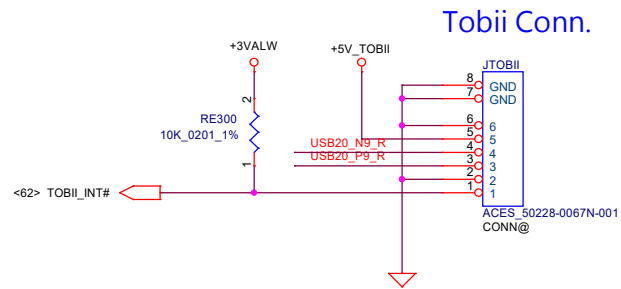
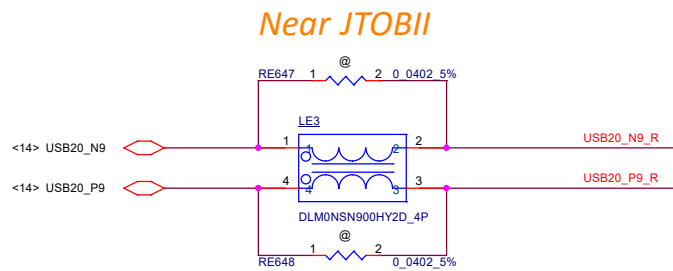
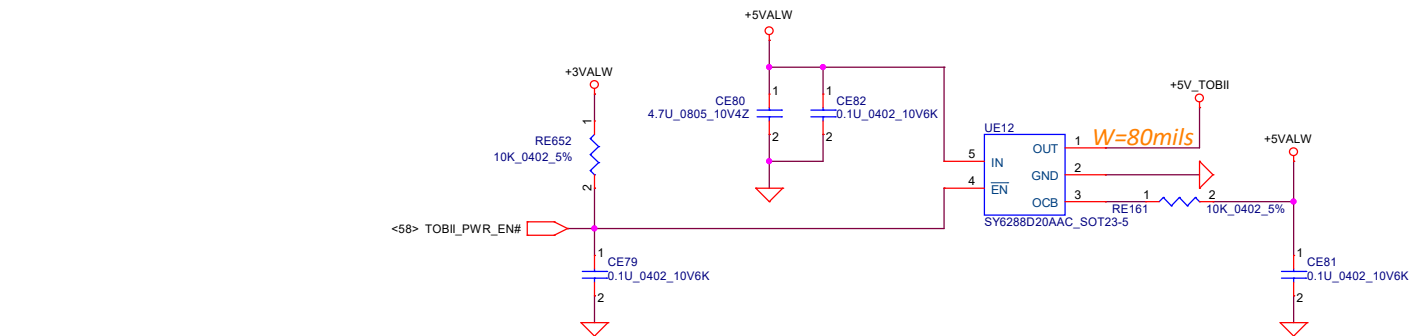


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Size	Document Number	Rev		1.0	
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A	B	C	D	E																								
1																												
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<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2018/03/29</td><td>Deciphered Date</td><td>2019/03/29</td><td colspan="2">Title Reserved</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size LA-G881P</td><td>Rev 1.0</td></tr><tr><td colspan="2">Date: Tuesday, January 08, 2019</td><td colspan="4">Sheet 73 of 101</td></tr></table>					Security Classification	Compal Secret Data			Compal Electronics, Inc.		Issued Date	2018/03/29	Deciphered Date	2019/03/29	Title Reserved		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size LA-G881P	Rev 1.0	Date: Tuesday, January 08, 2019		Sheet 73 of 101			
Security Classification	Compal Secret Data			Compal Electronics, Inc.																								
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A	B	C	D	E																								



Tie 1k ohm to VDD = Register Access SMBus Slave mode
 FLOAT = Read External EEPROM (Master SMBUS Mode)
 Tie 1k ohm to GND = Pin Mode

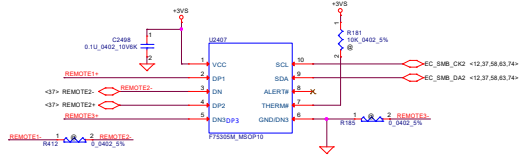


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				Size Document Number
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5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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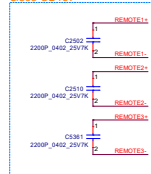
Fintek thermal sensor



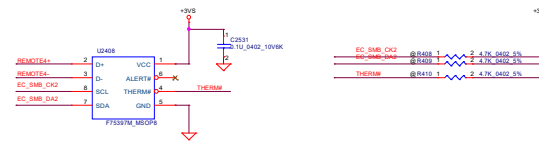
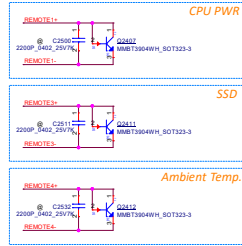
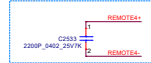
Address 1001_101b

REMOTE1,2,3,4 (+/-) :
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Trace length:<8"

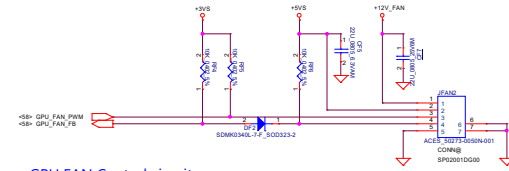
Close U2407



Close U2408



CPU FAN Control circuit



GPU FAN Control circuit

Power ON circuit

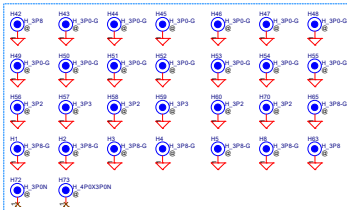
Power Button-TOP side



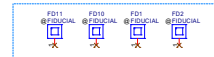
Power Button-BOT side



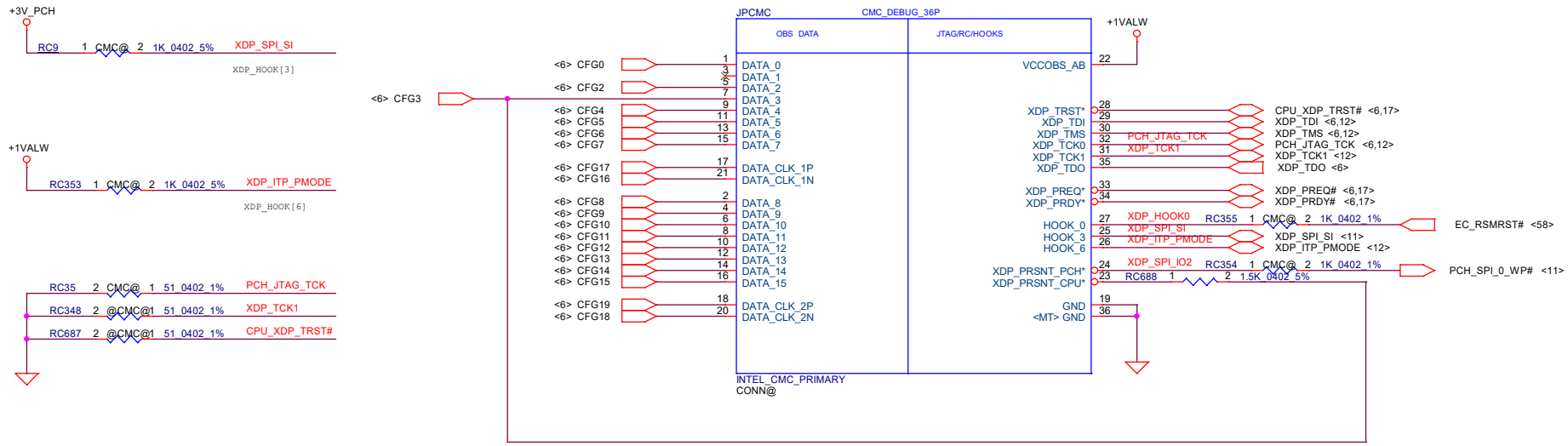
PCB Screw Hole



Fiducial Mark



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PWRTN/Thermal/SCREW/FAN				1.0
LA-G881P				Rev
Date: 2018/03/29				1.0



5

4

3

2

1

D

C

B

A

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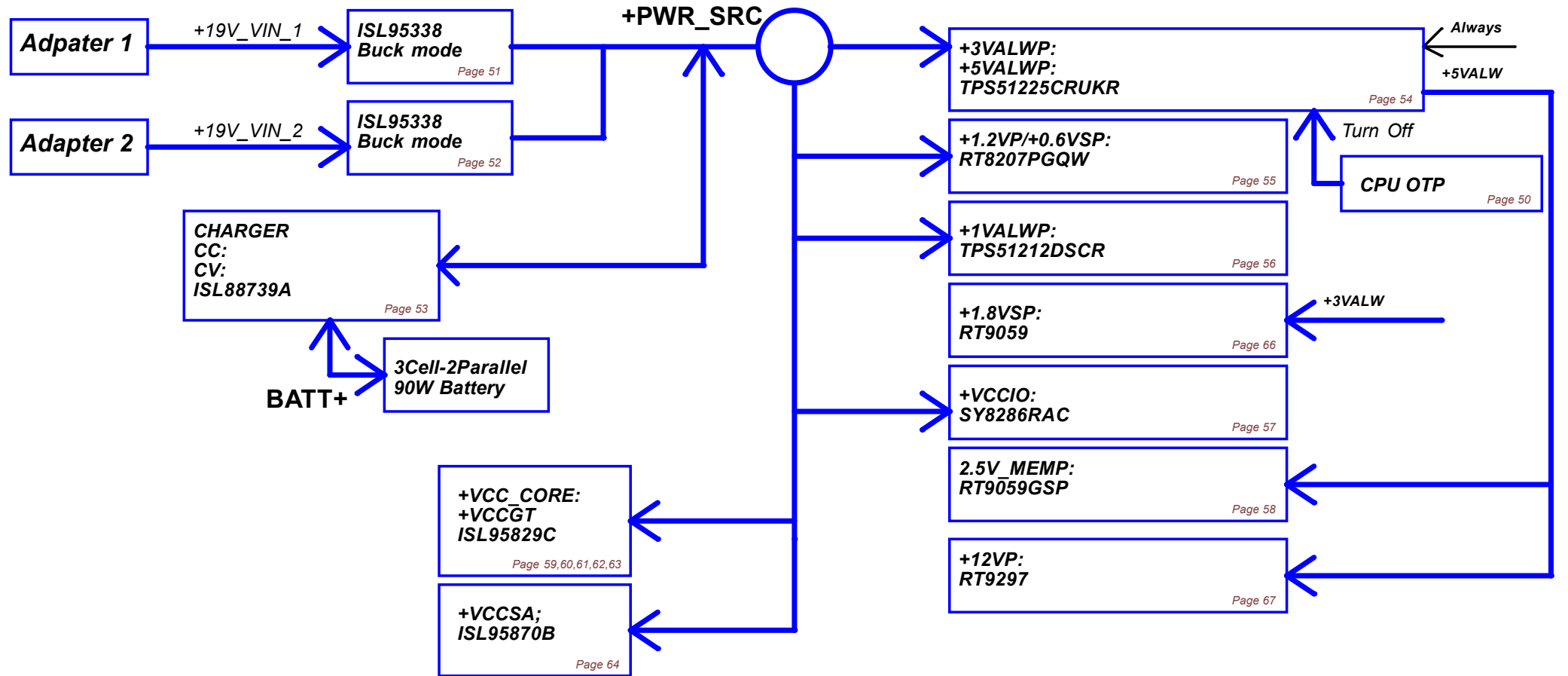
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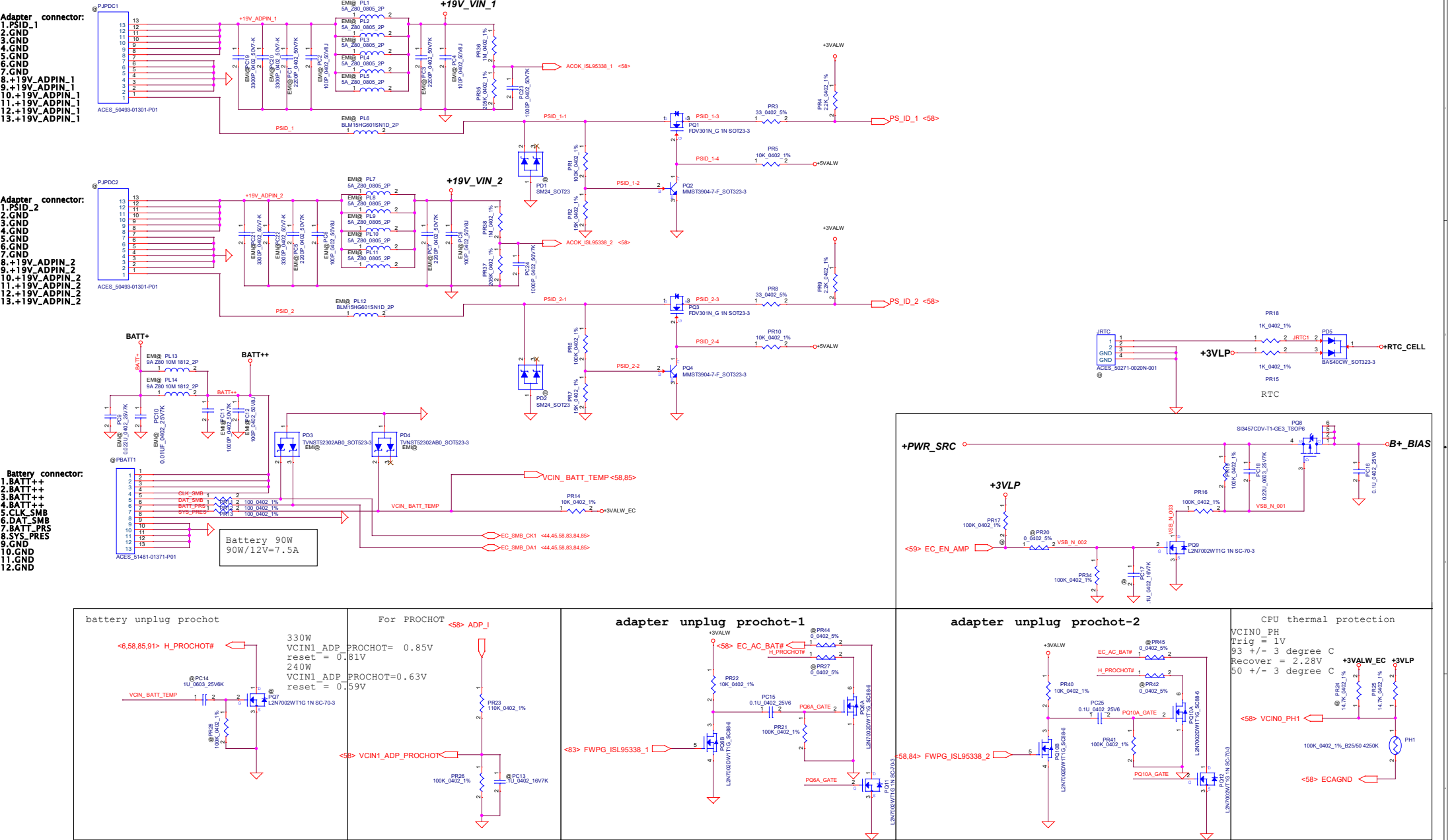
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1

Power block



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Adapter connector:
1.PSID_1
2.GND
3.GND
4.GND
5.GND
6.GND
7.GND
8.+19V_ADIPIN_1
9.+19V_ADIPIN_1
10.+19V_ADIPIN_1
11.+19V_ADIPIN_1
12.+19V_ADIPIN_1
13.+19V_ADIPIN_1

Adapter connector:
1.PSID_2
2.GND
3.GND
4.GND
5.GND
6.GND
7.GND
8.+19V_ADIPIN_2
9.+19V_ADIPIN_2
10.+19V_ADIPIN_2
11.+19V_ADIPIN_2
12.+19V_ADIPIN_2
13.+19V_ADIPIN_2

Battery connector:
1.BATT+
2.BATT+
3.BATT+
4.BATT+
5.CLK_SMB
6.DAT_SMB
7.BATT_PRES
8.SYS_PRES
9.GND
10.GND
11.GND
12.GND

Battery 90W
90W/12V=7.5A

battery unplug prohot

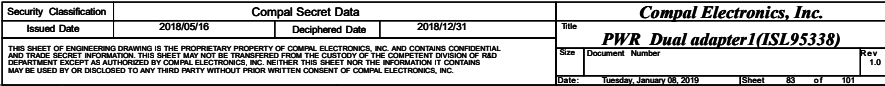
For PROCHOT

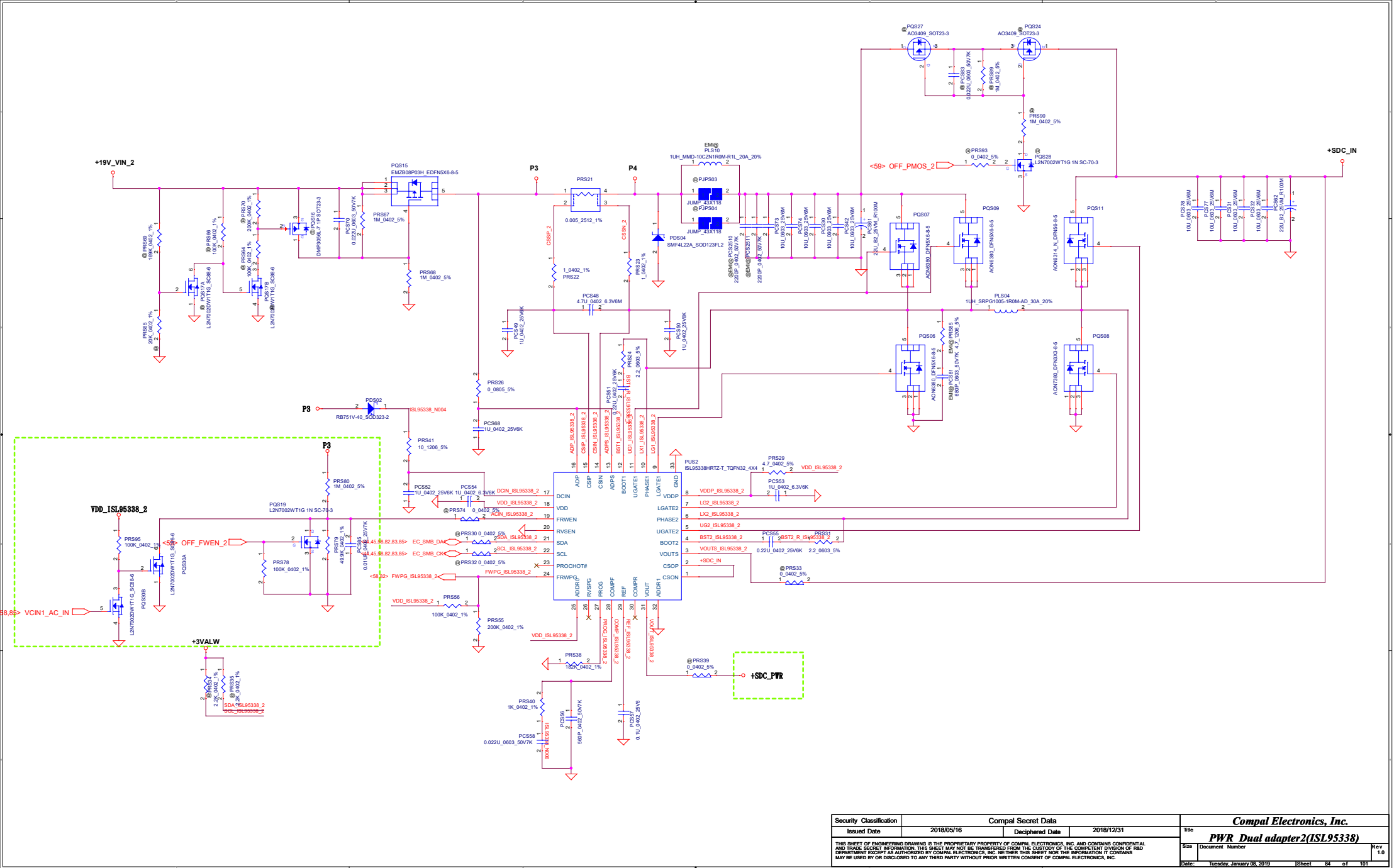
adapter unplug prohot-1

adapter unplug prohot-2

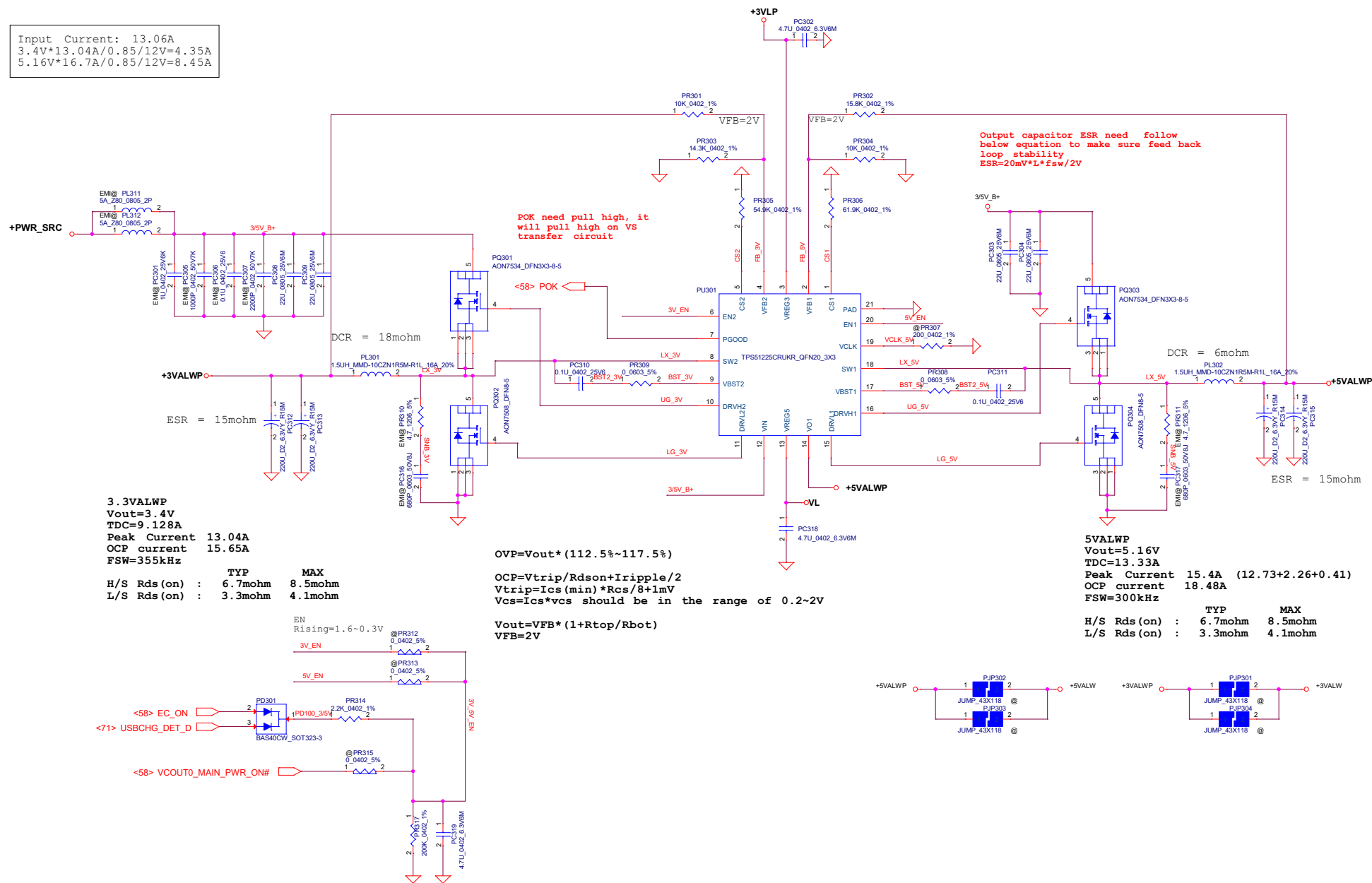
CPU thermal protection

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Title		Compal Electronics, Inc.	
Size		PWR_DC/BATT Conn/OTP/RTC	
Date		Tuesday, January 08, 2019	
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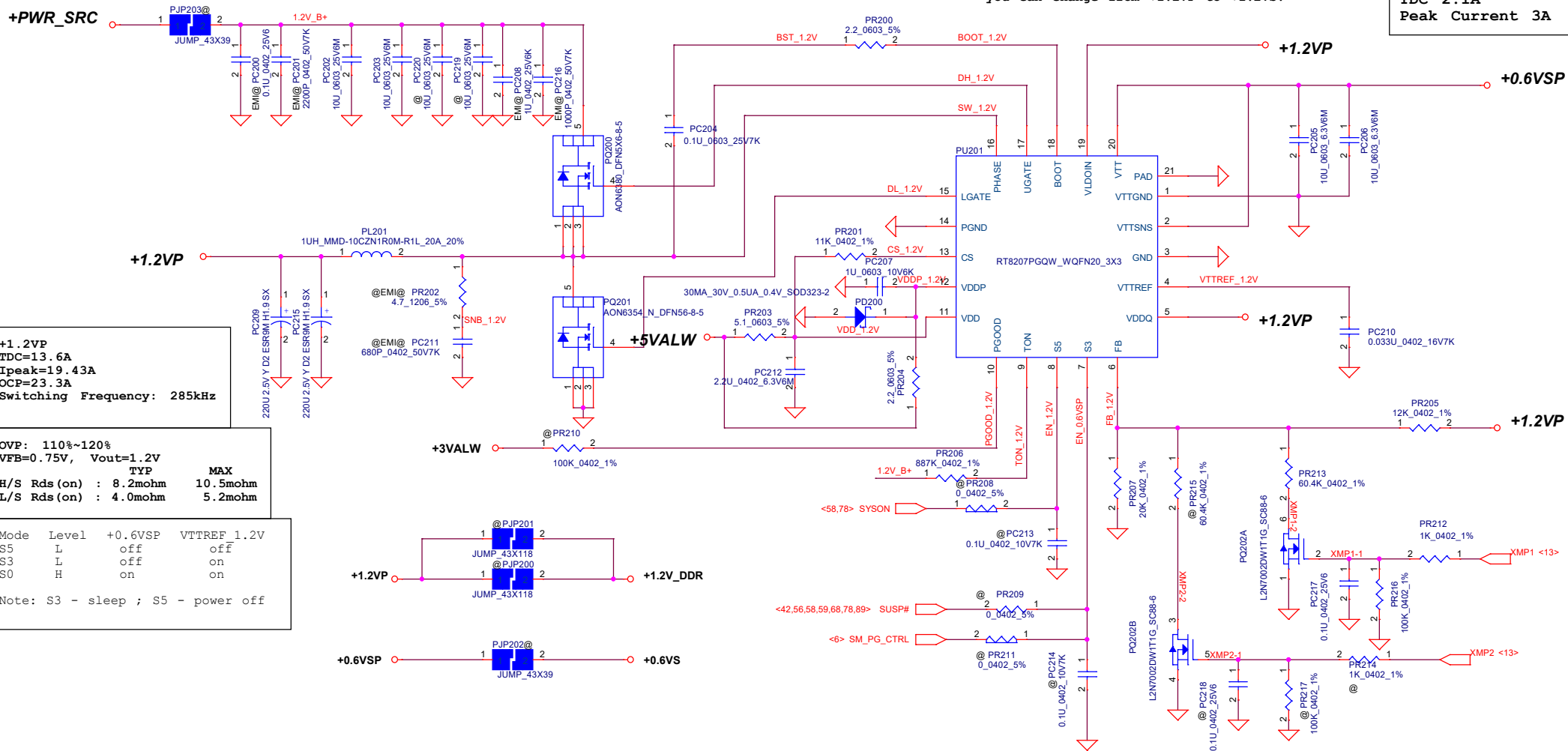




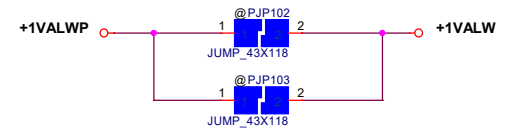
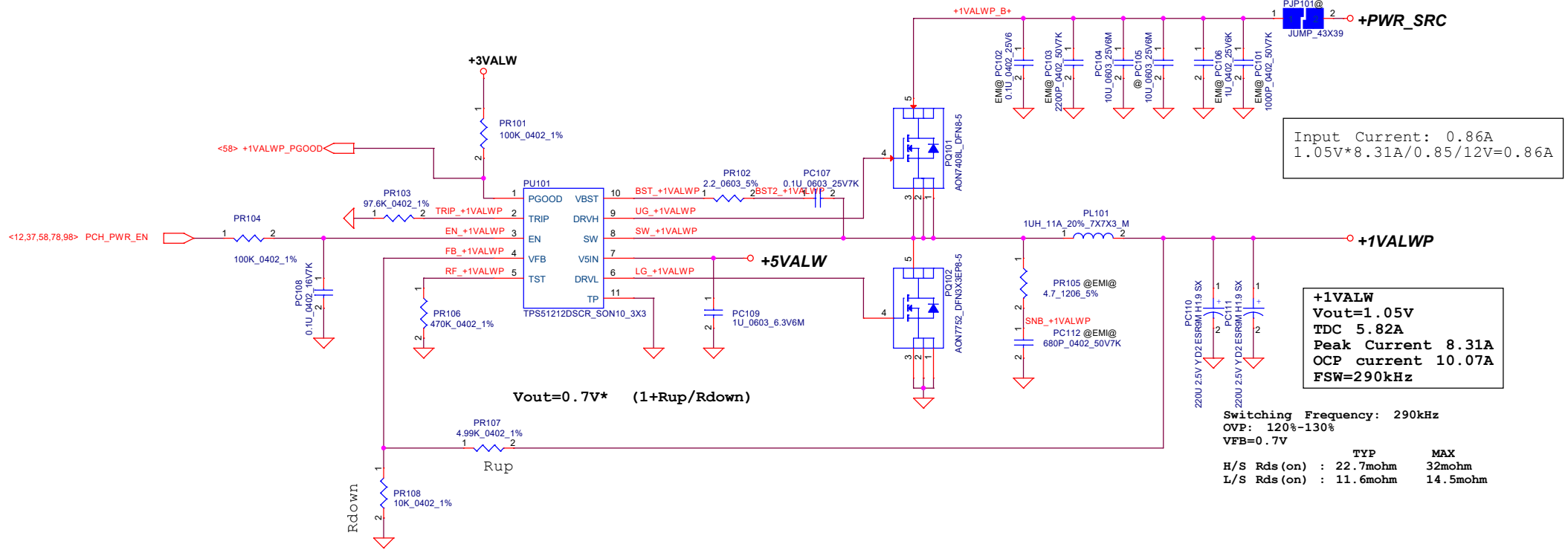
Input Current: 13.06A
 $3.4V \times 13.04A / 0.85 / 12V = 4.35A$
 $5.16V \times 16.7A / 0.85 / 12V = 8.45A$



Input Current: 1.17A
 $1.2V \cdot 9.93A / 0.85 / 12V = 1.17A$

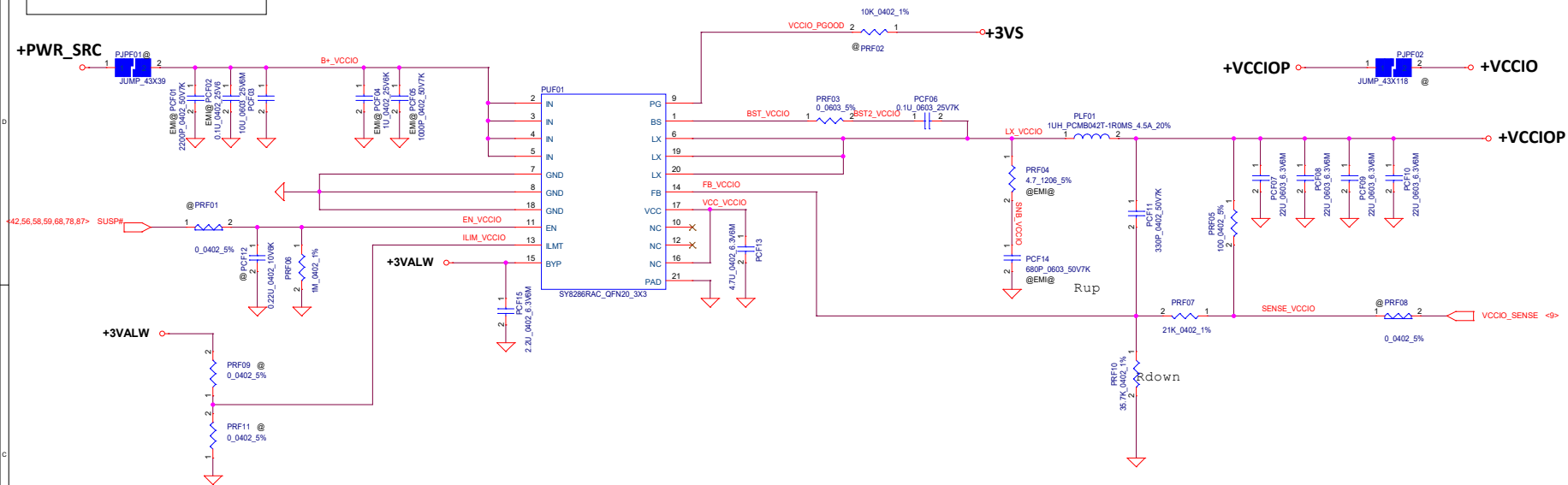


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Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title PWR 1.2VP/0.6VSP		
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				Size	Document Number	Rev
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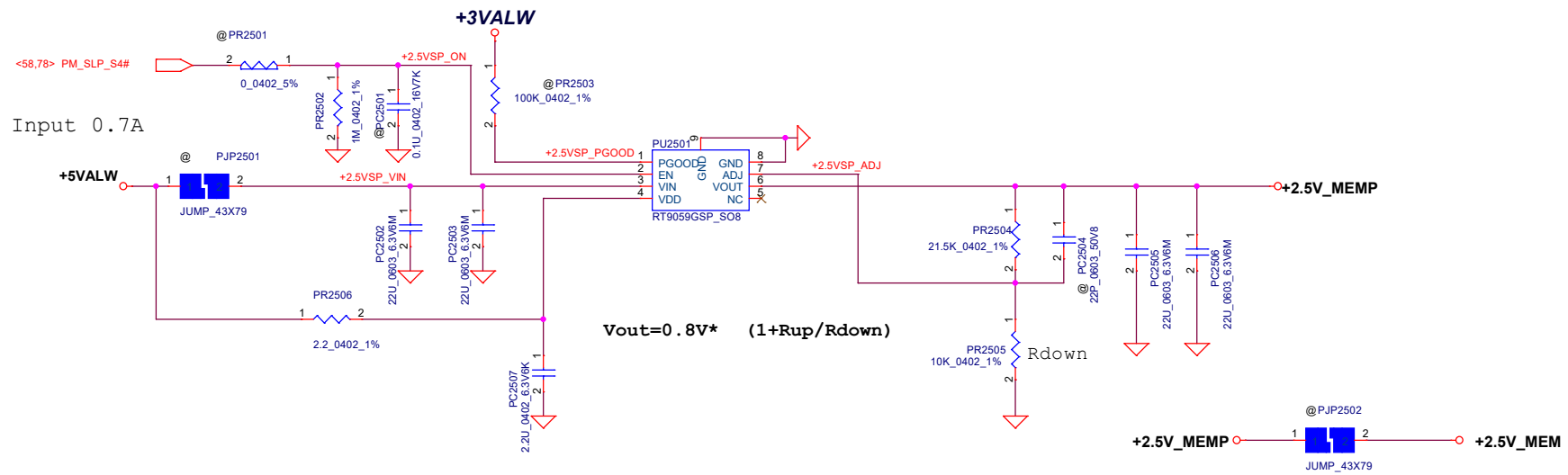
Input Current: 0.6A
 $0.95V \times 6.4A / 0.85 / 12V = 0.6A$



+VCCIOP (0.95V)
TDC 4.48 A
Peak Current 6.4 A
OCP Current 9 A Fix by IC
TYP MAX
Choke DCR 24.0mohm , 27.0mohm

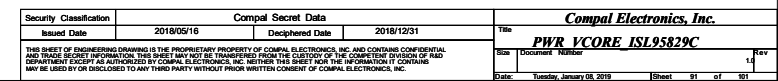
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				Date:	Tuesday, January 08, 2019	Sheet 89 of 101

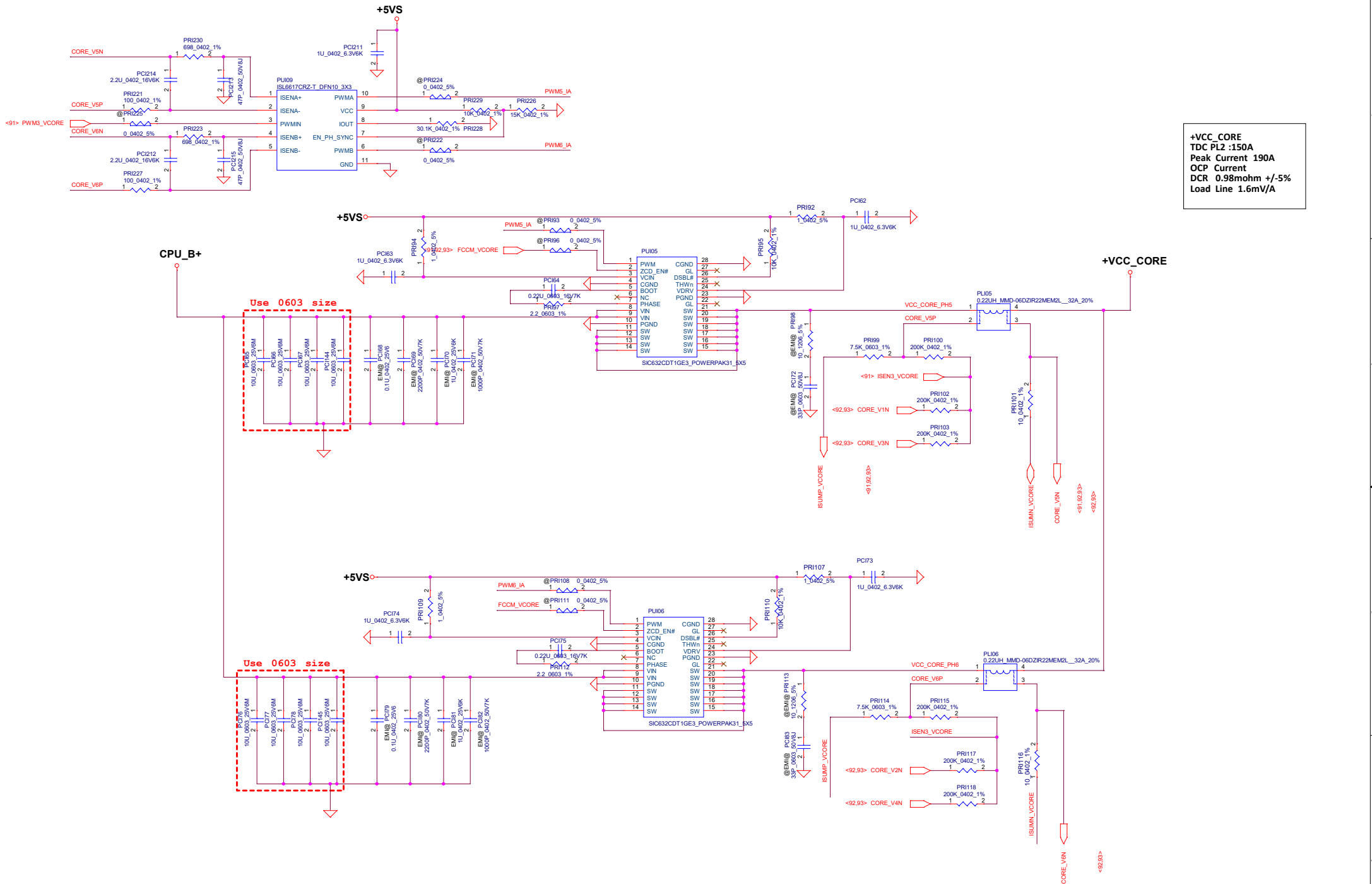
Input Current: 0.41A
 $2.5V \cdot 0.7A / 0.85 / 5V = 0.41A$



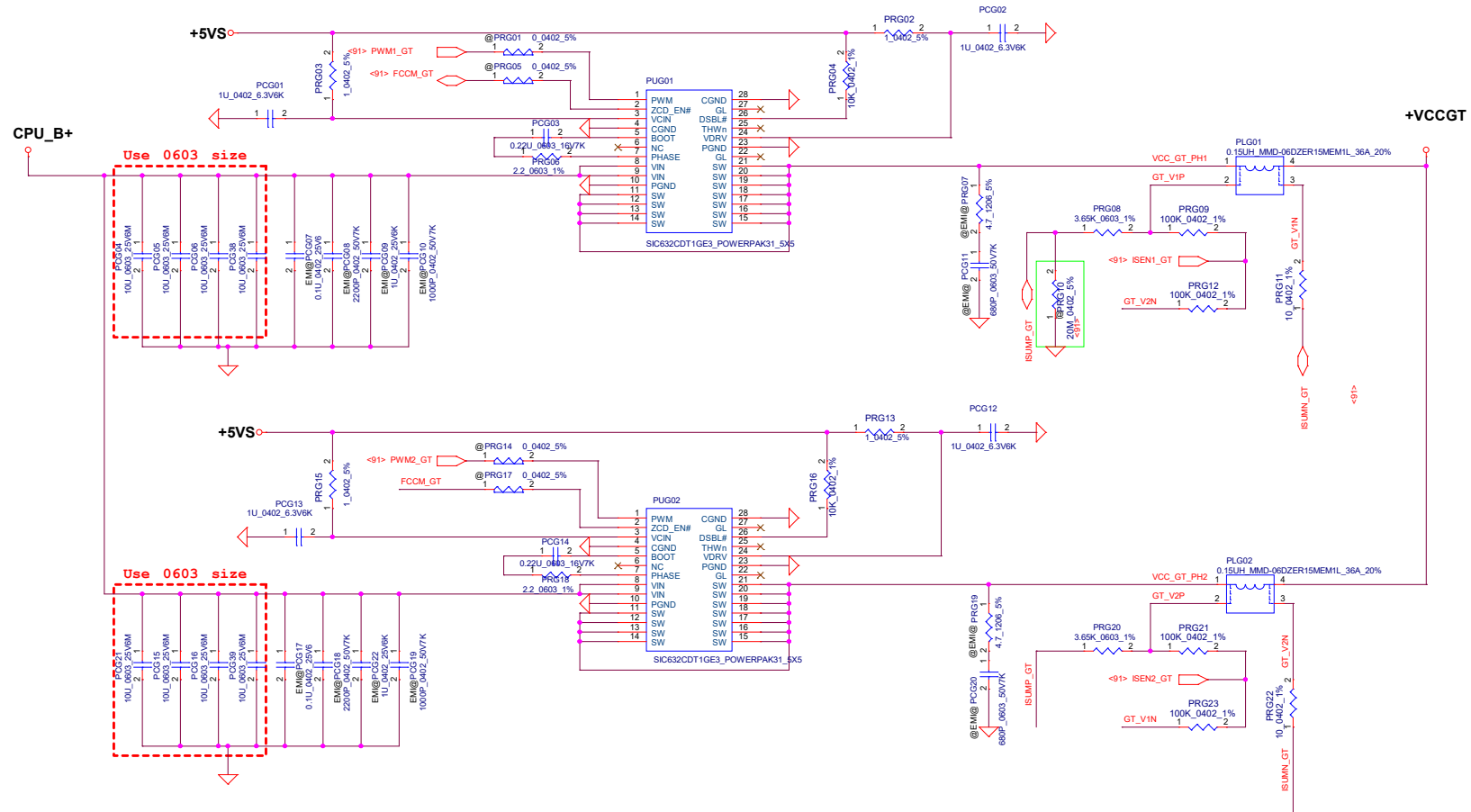
```
+2.5V MEM
TDC 0.49A
Peak Current 0.7A
OCP Current 3.5A
```

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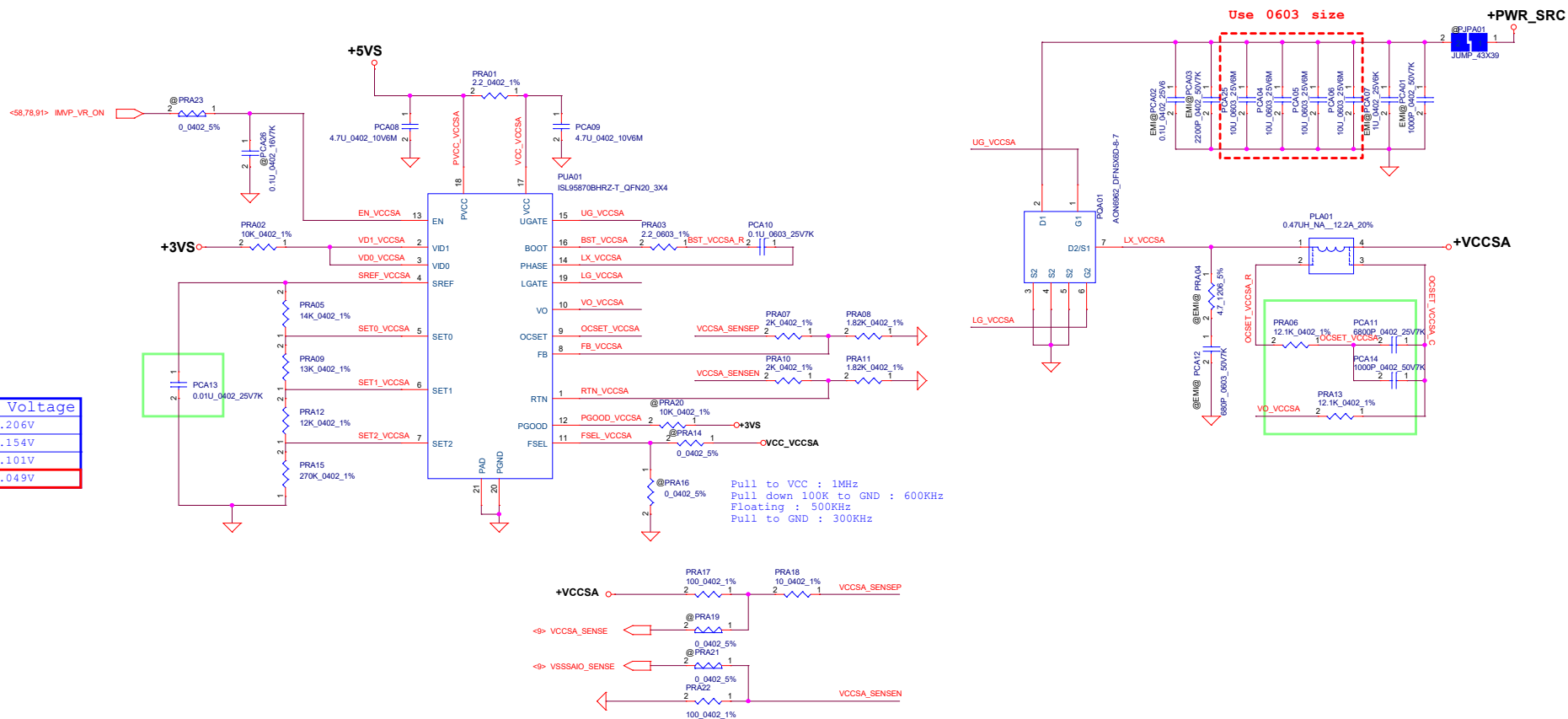


+VCCGT
TDC PL2 :30A
Peak Current 45A
OCP Current
DCR 0.67mohm +/-5%
Load Line 3.1mV/A

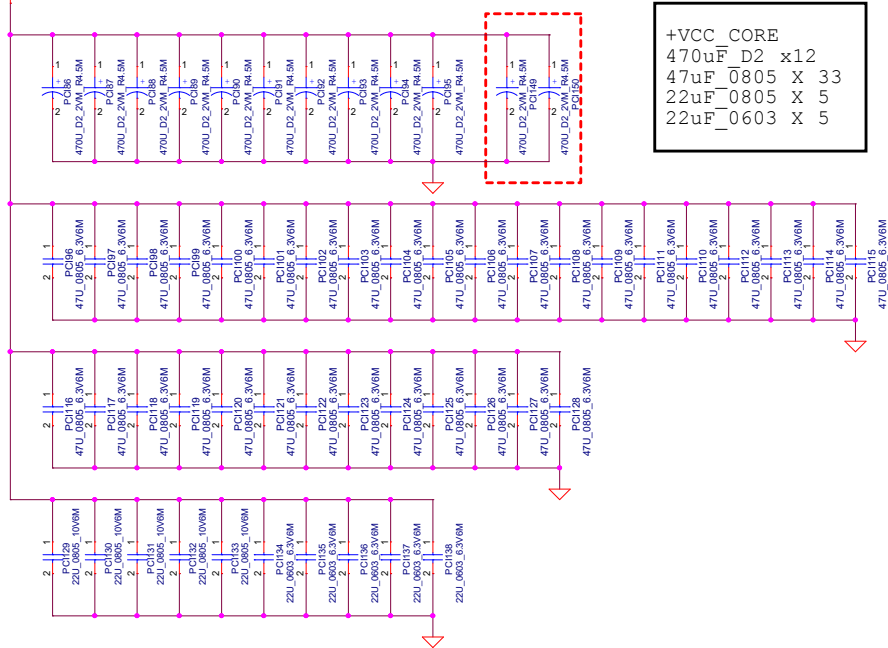


+VCCSA
TDC 10A
Peak Current 11.1A
OCP Current 13.32A
DCR 6.2mohm +/-5%

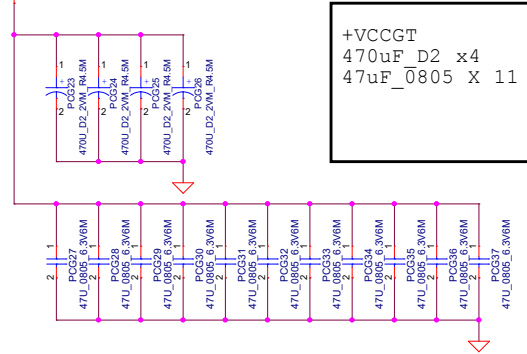
VID1	VID0	Output Voltage
0	0	1.206V
0	1	1.154V
1	0	1.101V
1	1	1.049V



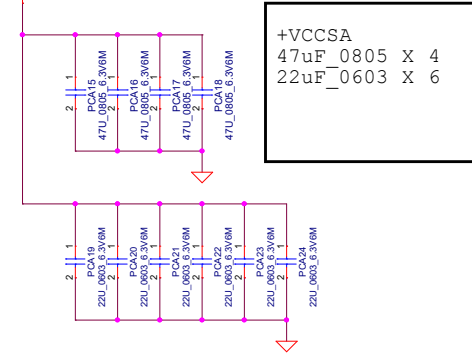
+VCC_CORE



+VCCGT

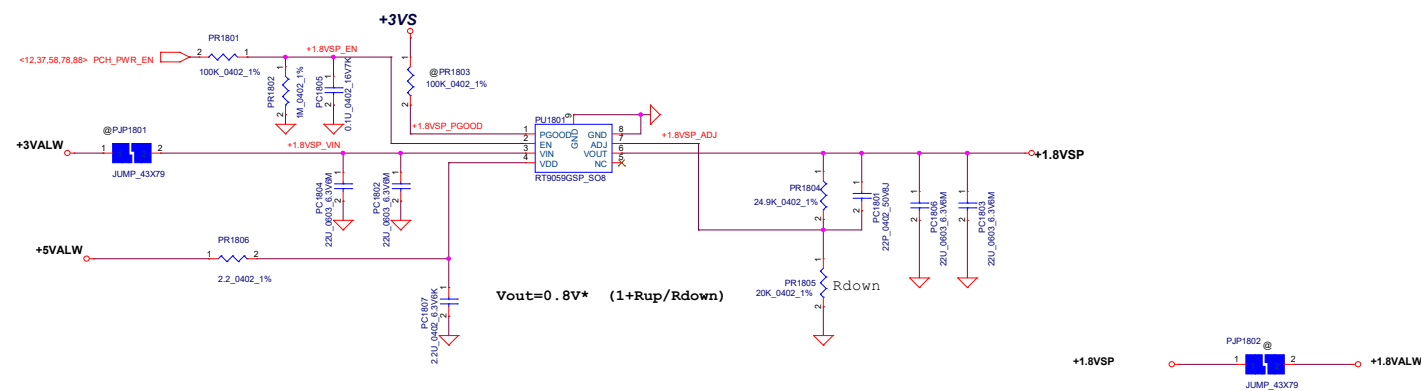


+VCCSA



Input Current: 0.03A
 $1.8V \times 0.18A / 0.85 / 3 = 0.127A$

+1.8VSP
TDC 0.13A
Peak Current 0.18A
OCP current 3.5A



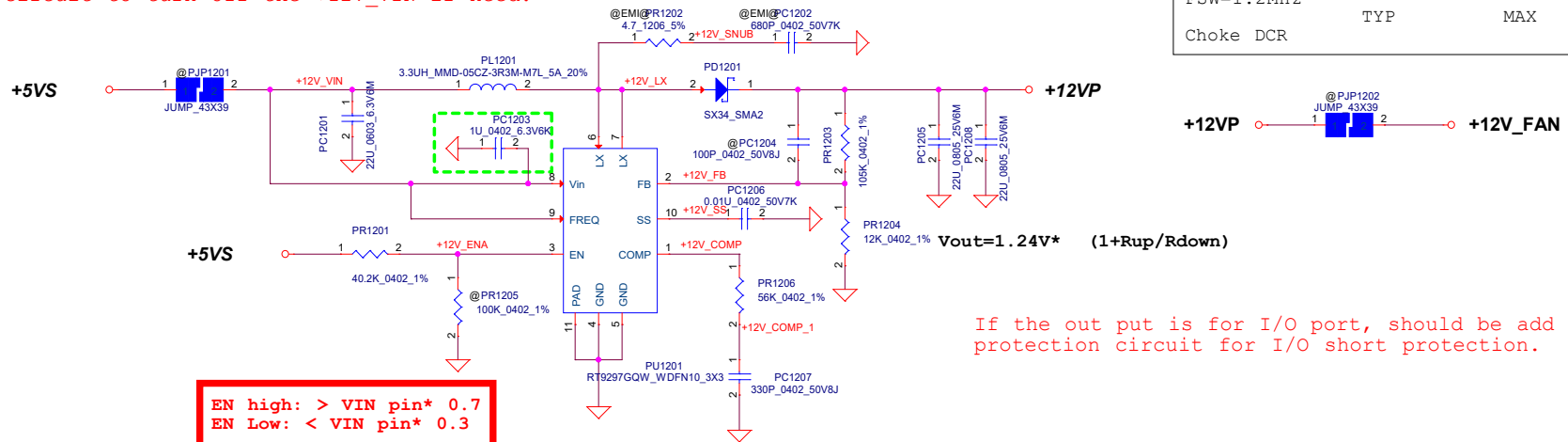
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Input Current: 2.26A
 $12V \times 0.8A / 0.85 / 5V = 2.26A$

+1.2VP
 TDC 0.56A
 Peak Current 0.8A
 OCP current 3A
 FSW=1.2MHz
 Choke DCR TYP MAX

Add a switch circuit to turn off the +12V_VIN if need.

Must check PL1201 and PD1201 rating for your application.



FREQ high : Frequency = 1.2MHz
 FREQ low : Frequency = 640KHz

If the out put is for I/O port, should be add protection circuit for I/O short protection.

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